PAW3805EK-CJV2: Track-On-Glass Mouse Chip

General Description

The PixArt PAW3805EK-CJV2 is an optical chip which is optimized for blue LED based wireless mouse application. It has high accuracy navigation ability that enables navigation virtually on any flat surface, including the transparent glass. The low power architecture and automatic power management make it suitable for power-sensitive application such as a wireless mouse. PAW3805EK-CJV2 is capable of high-speed motion detection up to the velocity of 40 inches/sec and 10g on non-glass surfaces, 20 inches/sec and acceleration of 5g on glass surface. In addition, it has an on-chip oscillator and a built-in programmable LED current driver. In order to achieve the best tracking performance, it is recommended to match the chip with L029-SSI optical lens.

Key Features

- Integrated package with optical chip and light source
- Virtually track on any flat surface, including glass
- Ultra-low power consumption
- Interface : 3-wire SPI (NCS, SCLK, SDIO)
- 16-bit motion data length for X-movement and Y-movement
- Resolution up to 3000cpi with ~26cpi per step
- Motion detection interrupt output
- Built-in Low Power Timer (LPT) for Sleep1/ Sleep2/ Sleep3 mode
- Programmable downshift time and sampling time during sleep modes
- Adaptive frame rate control for power saving during moving at different speeds
- Programmable LED Current Source (5-bits with 1.2mA/step) to provide LED with constant current

Applications

- Wireless mouse applications
- Optical navigation systems

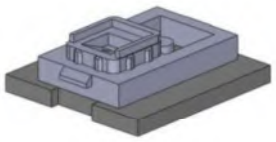
Key Parameters

Parameter	Value
Supply Voltage (V)	2 VDD Voltage Segments: High segment: 2.1 - 3.3V Low segment: 1.7 - 1.9V
	VLED : 3.3V (for blue LED)
Interface	3-wire SPI (NCS, SCLK, SDIO)
Light Source	Blue 470 nm wavelength
Companion Lens	L029-SSI
Tracking Speed (ips)	Up to 40 on non-glass surfaces Up to 20 on glass surface
Acceleration (g)	Non-Glass surfaces: 10 (max.) Glass surface: 5 (max.)
Resolution (cpi)	Up to 3000 (~26 per step)
Operating Current @ VDD = 3.3V, on glass surface	Run : 2.5 mA Sleep1 : 500 µA Sleep2 : 80 µA Sleep3 : 40 µA Power down : 15 µA
Package Dimension L x W x H (mm)	10.7 x 9.8 x 3.67

Ordering Information

Part Number	Package Type
PAW3805EK-CJV2	LGA 12-pin
L029-SSI	Trim Lens

RoHS compliant



For any additional inquiries, please contact us at
http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

PAW3805EK-CJV2 is a high performance and ultralow power CMOS-processed optical image chip with integrated digital image process circuits. It is based on an optical navigation technology which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, the direction and the magnitude of motion. The movement Delta_X and Delta_Y information are available in registers which are accessible through 3-wire SPI serial interface. A host controller reads and translates the data from the SPI interface into RF signals before sending them to the host PC.

PAW3805EK-CJV2 is designed to work on glass (including the transparent glass) with thickness of at least 4mm. Most glass surfaces provide enough microscopic features to enable motion tracking. It will not work on the glass which is perfectly clean and virtually scratch-free. The minimum requirements for PAW3805EK-CJV2 to work reliably on glass is there must be at least 44 features/mm^2 at the minimum of 5µm width and 2µm depth. Basically, PAW3805EK-CJV2 is able to virtually navigate on any flat surfaces.

The Figure 1 below shows the architecture block diagram of the chip. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks. This datasheet describes the electrical characteristics, switching characteristics, introduction to different functions and the register settings of PAW3805EK-CJV2.

Note: Throughout this document PAW3805EK-CJV2 is referred to as the chip.

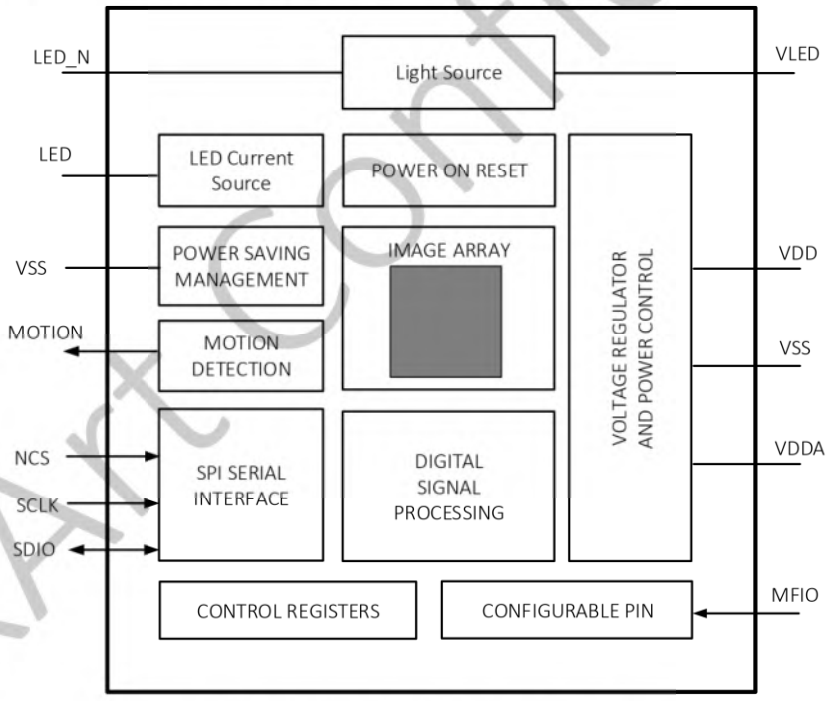


Figure 1. Chip Architecture Functional Block Diagram

1.2 Terminology

Term	Description
IPS	Inches per Second
FPS	Frame per Second
TOG	Track on Glass
CPI	Counts per Inch
SPI	Serial Peripheral Interface
LGA	Land Grid Array

1.3 Signal Description

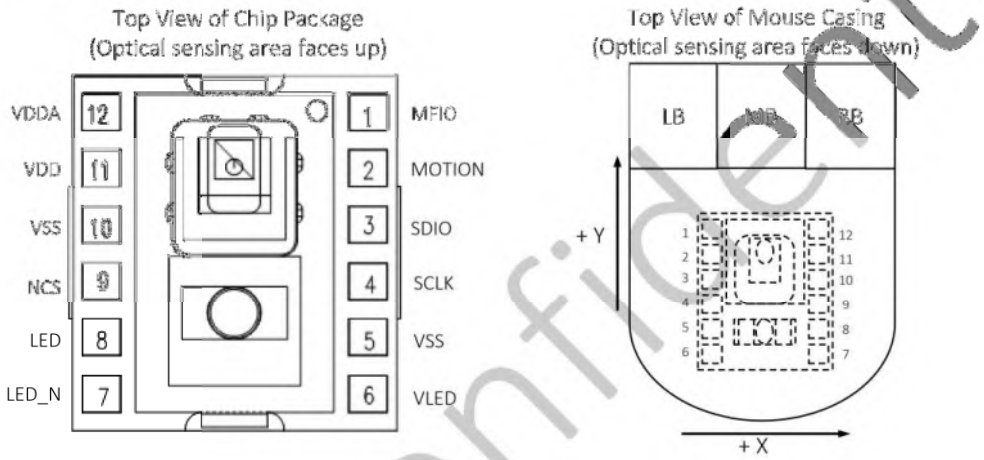


Figure 2. Pinout Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
1	MFIO	IN	Multi-functional I/O pin (can be programmed to the functions below): ▪ RST (Reset): Active high to reset the whole chip ▪ QB (Quick-Burst): To quickly read out motion data ▪ PD (Power Down): Active high to force the chip enter power down mode ▪ NF (Null Function) : Power-up default
2	MOTION	OUT	Motion detection output (active low)
3	SDIO	I/O	Bi-direction I/O for 3-wire SPI
4	SCLK	IN	Clock input for 3-wire SPI
5	VSS	GND	Chip ground
6	VLED	PWR	Power supply input for LED (3.3V power for blue LED)
7	LED_N	PWR	LED Cathode, should be connected to LED pin
8	LED	PWR	LED control pin, should be connected to LED_N pin
9	NCS	IN	NCS: chip select pin (active low) in SPI mode
10	VSS	GND	Chip ground
11	VDD	PWR	Power supply input
12	VDDA	PWR	High voltage segment (VDD: 2.1V ~ 3.3V): VDDA is 1.8V regulator output and should connect a 1uF capacitor to ground Low voltage segment (VDD: 1.7V ~ 1.9V): VDDA should connect to VDD directly

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
DC Supply Voltage	V_{DC}	-0.3	3.9	V	High Voltage Segment
		-0.2	2.3	V	Low Voltage Segment
I/O Voltage	V_{IO}	-0.3	V_{DC}	V	All I/O pin
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model JESD22-A114E with 15 sec zap interval.

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
4. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0	25	40	°C	
Storage Temperature	T_{STG}	-40	-	85	°C	
Power Supply Voltage	VDD	1.7	1.8	1.9	V	High Voltage Segment
		2.1	2.7	3.3	V	Low Voltage Segment
	VLED	-	3.3	-	V	LED Power for Blue LED
Supply Noise (peak to peak)	V_{pp}	-	-	100	mV	Peak to peak voltage within 100KHz – 80MHz
SPI Clock Frequency	SCLK	-	-	2	MHz	
Tracking Speed	SP	0	-	40	IPS	@ non-glass surfaces
				20		@ glass surface
Tracking Acceleration	AC	0	-	10	g	@ non-glass surfaces
				5		@ glass surface

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Consumption on glass surface	I_{DDNM}	-	2.5	-	mA	Run mode current. Based on 85% weighting for speed ≦5ips and 15% weighting for speed >5ips
	I_{DDS1}	-	500	-	µA	Sleep1 current, based on 8ms sampling period
	I_{DDS2}	-	80	-	µA	Sleep2 current, based on 128ms sampling period
	I_{DDS3}	-	40	-	µA	Sleep3 current, based on 512ms sampling period
	I_{DDPD}	-	15	-	µA	Power down current
I/O Input High Voltage	V_{IH}	0.7* V_{DD}	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.3* V_{DD}	V	
I/O Output High Voltage	V_{OH}	V_{DD} -0.4	-	-	V	@I_{OH} = 2mA
I/O Output Low Voltage	V_{OL}	-	-	0.4	V	@I_{OL} = 2mA

Notes: All the parameters are tested under operating conditions: V_{DD} = 3.3V (including LED current), T_A = 25°C

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
QB(Quick Burst) high pulse time	QB_{HIGH}	2	-	-	µs	
RST(Reset) high pulse time	RST_{HIGH}	500	-	-	µs	
3-wire SPI Speed	F_{SPI}	-	-	2	MHz	

Note: All the parameters are tested under operating conditions: V_{DD} = 3.3V, T_A = 25°C

3.0 Mechanical Specifications

3.1 Mechanical Dimension

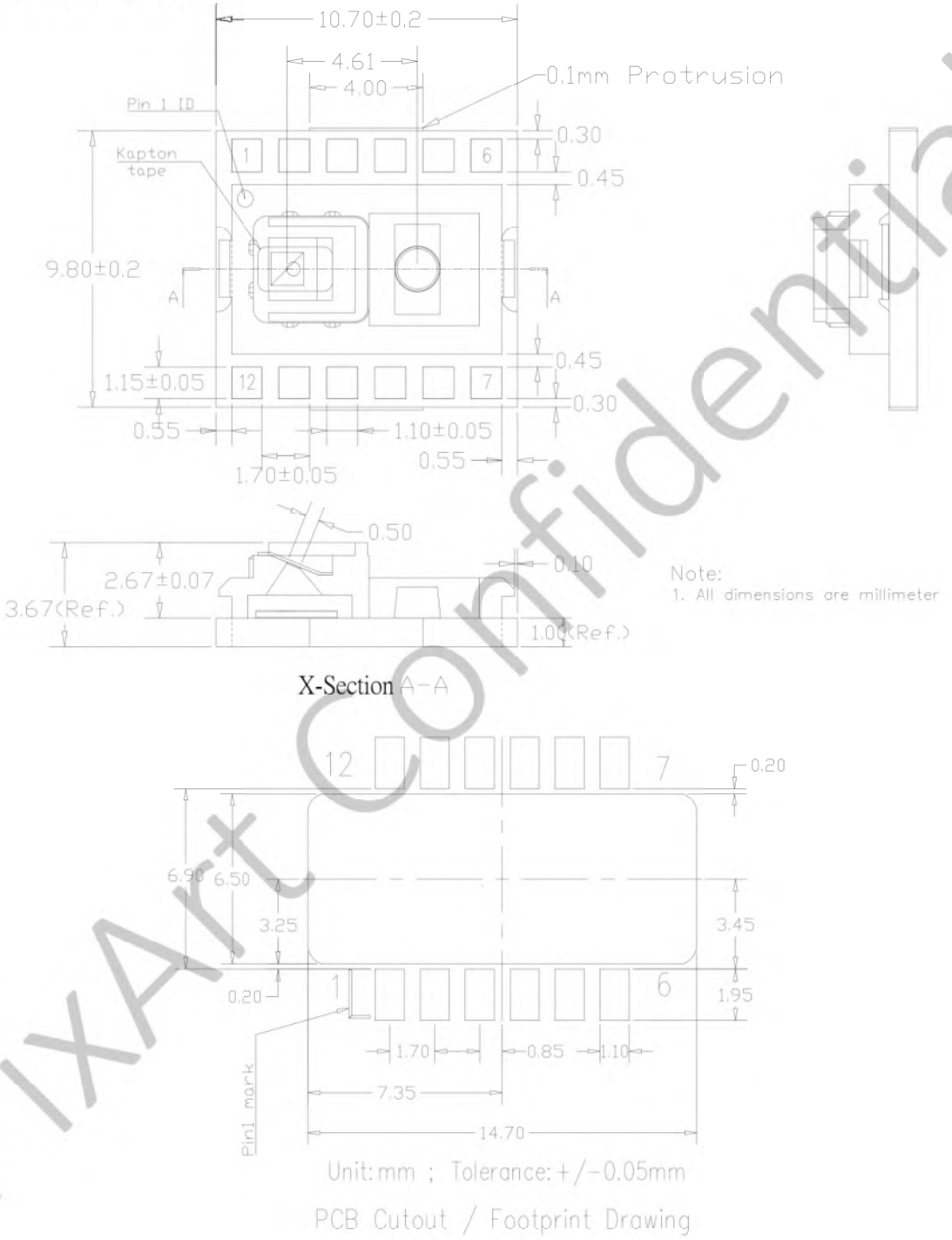


Figure 3. Chip Package Outline and PCB Cutout Drawings

3.2 Mechanical Assembly Drawings

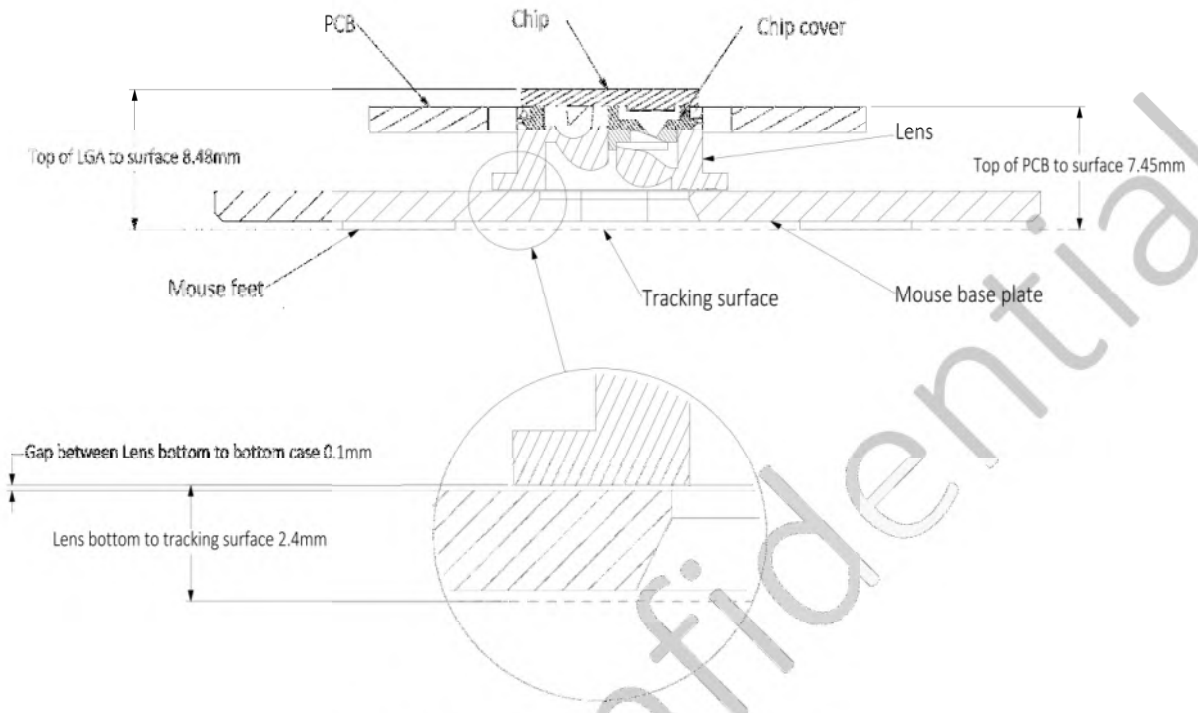


Figure 4. 2D Assembly of Chip, Lens, PCB and Base Plate

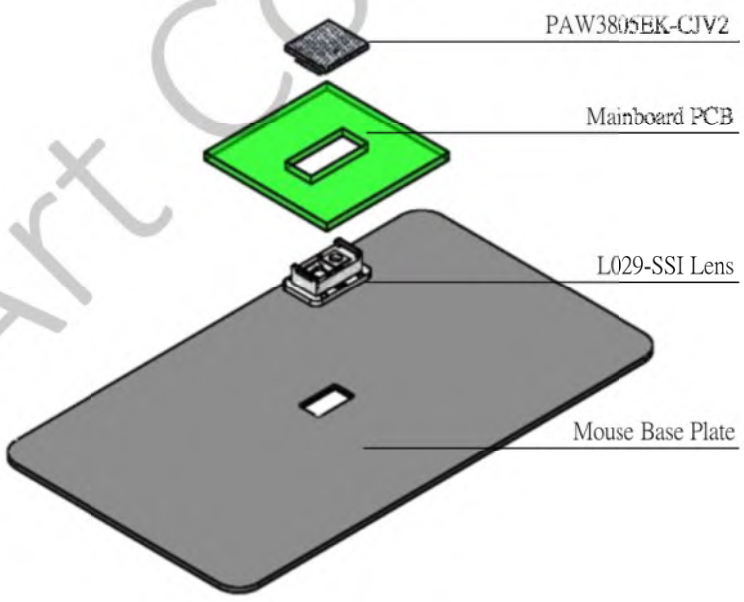


Figure 5. Exploded 3D Assembly View of Chip, Lens, PCB and Base Plate

4.0 Design Reference

4.1 Reference Application Schematics

The chip only supports simplified 3-wire SPI slave mode, while some host controllers may only support standard 4-wire SPI master mode. In this case, users can connect the host controller to the chip using the method shown below to communicate with each other. Take note that the 3.3K ohm resistor is for reference only and the resistance may have to be modified according to different I/O capability as per the specification of the host controllers.

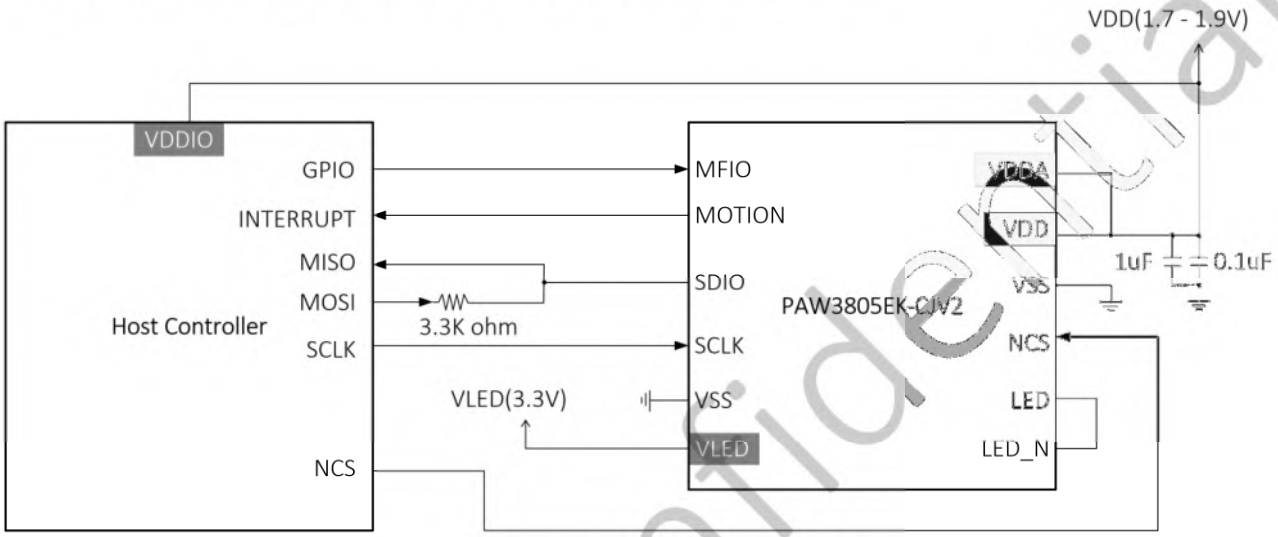


Figure 6. Application Circuit for Low Voltage Segment

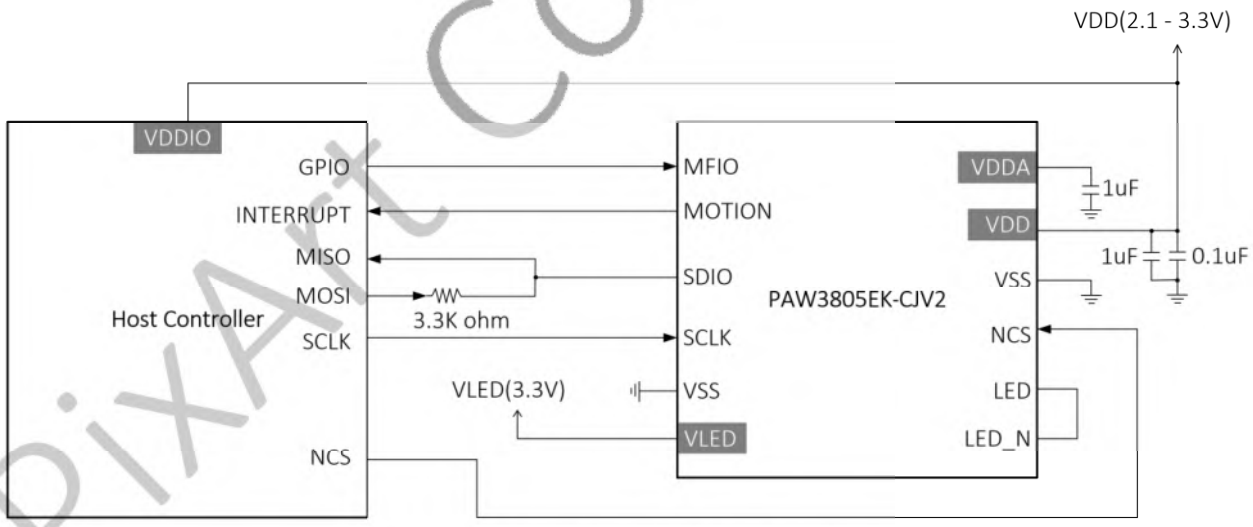


Figure 7. Application Circuit for High Voltage Segment

4.2 Power Supply Configuration

The chip has 2 voltage segments for power supply configuration, the High Voltage Segment and the Low Voltage Segment. These two segments provide flexibility to applications with different power considerations.

4.2.1 High Voltage Segment

The power supply voltage of High Voltage Segment ranges from 2.1V to 3.3V. The power pins connection of VDD and VDDA of the chip is shown in Figure 8.

- VDD is connected to the supply voltage with bypass capacitor of 0.1µF and 1µF.
- VDDA should be connected to 1µF bypass capacitor to VSS ground.

4.2.2 Low Voltage Segment

The power supply voltage of Low Voltage Segment ranges from 1.7V to 1.9V. The power pins connection of VDD and VDDA of the chip should be connected as shown in Figure 9.

- VDD and VDDA should be tied together and connected to the supply voltage with bypass capacitor of 0.1µF and 1µF to VSS ground.

The chip's default setting upon power-up is meant for the High Voltage Segment. When using the Low Voltage Segment, the custom registers setting as below should be written into the chip after the power-up reset. If these registers are not properly set, the chip would consume additional power due to the leakage current of the internal regulator.

- Write address 0x7F = 0x00; to change register bank 0
- Write address 0x09 = 0x5A; to disable Write Protect
- Write address 0x52 = 0x05; to turn off internal regulator for Low Voltage Segment
- Write address 0x09 = 0x00; to enable Write Protect

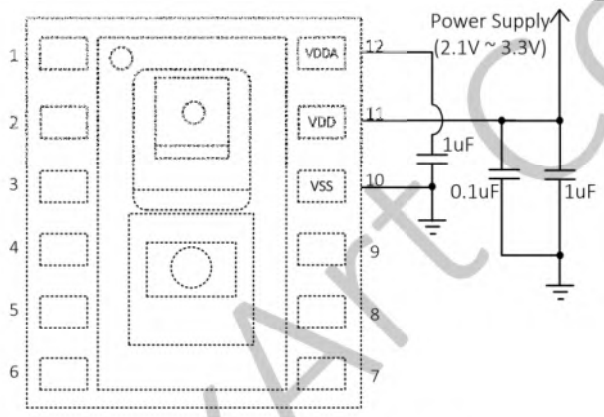


Figure 8. High Voltage Segment

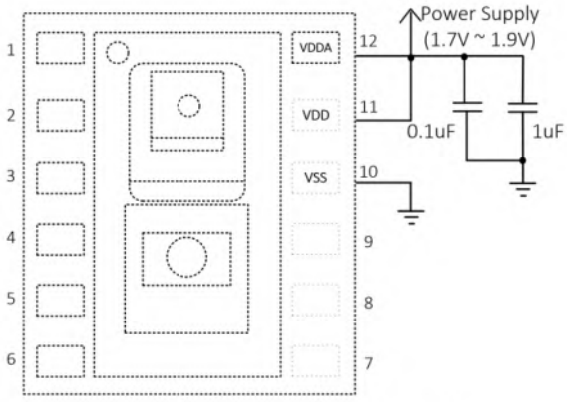


Figure 9. Low Voltage Segment

5.0 Sleep Modes for Power Saving

The chip has three power-saving modes: Sleep1, Sleep2 and Sleep3 (default is disabled, please refer to the descriptions of register address 0x06). Each mode has a different motion detection time to detect the motion periodically. When the chip is left idle, the chip automatically changes from Run mode to Sleep1 mode, then subsequently to Sleep2 mode and finally to Sleep3 mode.

When designing the power saving behavior of an application, do take note on the following considerations.

- **Current Consumption vs. Wake-up Time:** Sleep3 is consuming the least current among the three power saving modes. As the current consumption is the lowest in Sleep3 mode and being the highest in Sleep1 mode, adversely the time required for the chip to "wake up" and back to Run mode from Sleep1 mode is the shortest and being the longest from Sleep3 mode.
- **Sleep Entering Time:** Slp1_Etm, Slp2_Etm or Slp3_Etm is the elapsed time from the moment when the chip is idle and then going into Sleep1/ Sleep2/ Sleep3 modes.
- **Sampling Frequency Time:** Slp1_Freq, Slp2_Freq or Slp3_Freq is the time period which the chip is sampling to detect the motion under Sleep modes.

The relationship between the entering time and the sampling frequency time is shown in Figure 10.

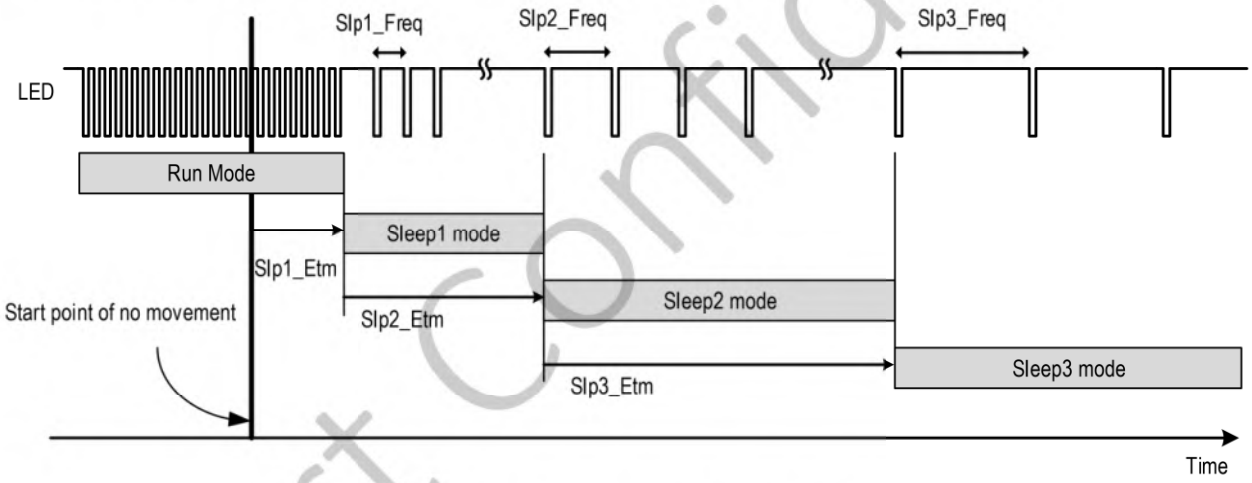


Figure 10. Sleep Modes for Power-Saving

6.0 3-Wire SPI Serial Interface

The chip supports 3-wire Serial Peripheral Interface (SPI). The host controller can use the SPI to write and read registers in the chip, and to read out the motion information. The host controller always initiates communication; the chip never initiates data transfers. NCS, SCLK and SDIO may be driven directly by the host controller. SDIO may also be driven by the chip when data is read out from chip's registers.

- NCS: Chip select input (active low). NCS needs to be low to activate the SPI; otherwise, SDIO will be at high-Z state and SCLK will be ignored. NCS can also be used to reset the SPI in case a communicational error happens.
- SCLK: Clock input. It is always generated by the host controller.
- SDIO: Bi-directional input/output data

6.1 Transmission Protocol

The transmission protocol is a 3-wire link, half duplex protocol between the host controller and the chip. All data changes on SDIO are initiated by the falling edge on SCLK. The host controller always initiates communication; the chip never initiates data transfers. The transmission protocol consists of the following two operation modes:

- Write Operation
- Read Operation

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit-7 as its MSB to indicate data direction. The second byte contains the data.

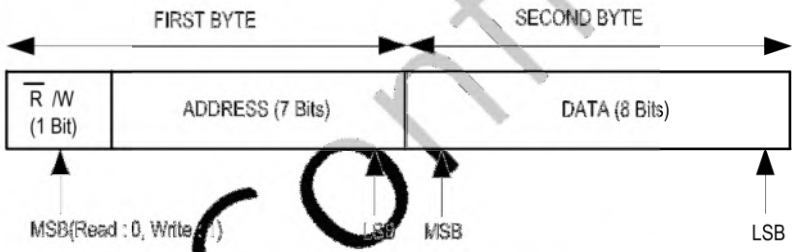


Figure 11. Transmission Protocol

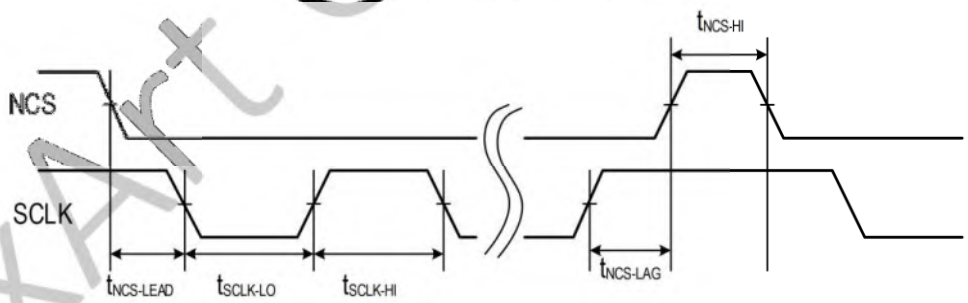


Figure 12. NCS vs SCLK Timing Requirement

6.1.1 Write Operation

A write operation, defined as data is going from the host controller to the chip, is always initiated by the host controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The communication is synchronized by SCLK. The host controller changes SDIO on the falling edges of SCLK and the chip reads SDIO on the rising edges of SCLK.

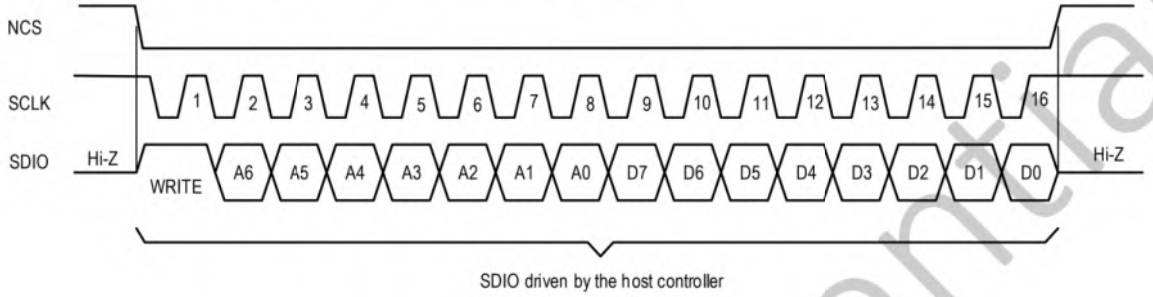


Figure 13. Write Operation

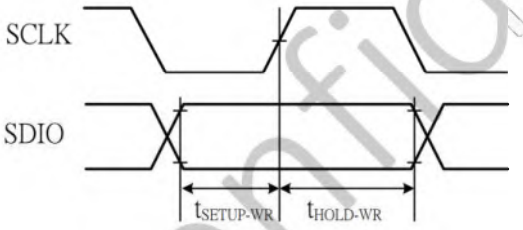


Figure 14. SDIO setup and hold time during write operation

6.1.2 Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains the address specified by the host controller and has a "0" as its MSB to indicate data direction. The second byte contains the data which is outputted by the chip. The communication is synchronized by SCLK. SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. The host controller must release SDIO bus and handover the control of SDIO bus to the chip on the falling edge of last address bit.

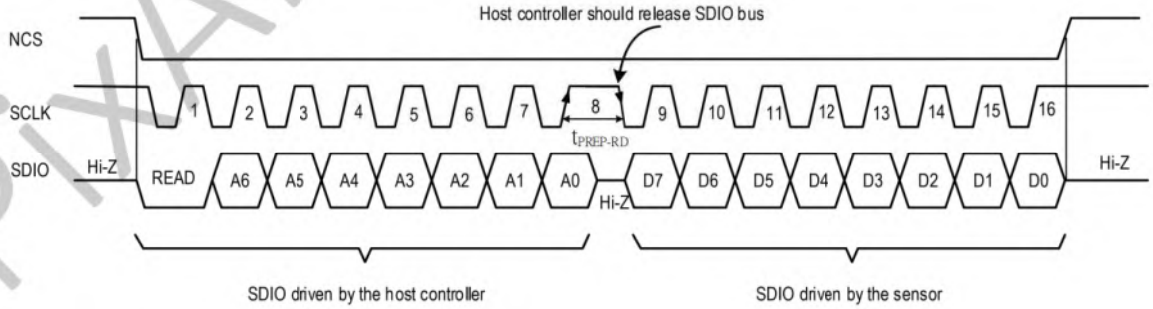


Figure 15. Read Operation

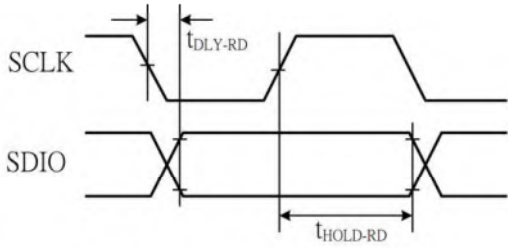


Figure 16. SDIO delay and hold time during read operation

6.2 SPI Timing

Table 6. SPI Timing Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCLK frequency	F_{SCLK}	-	-	2	MHz	SPI max. operation frequency
SCLK High Time	$t_{SCLK-HI}$	250	-	-	ns	SCLK min. high time
SCLK Low Time	$t_{SCLK-LO}$	250	-	-	ns	SCLK min. low time
NCS Enable Lead Time	$t_{NCS-LEAD}$	1	-	-	µs	From NCS falling to first SCLK falling
NCS Enable Lag Time	$t_{NCS-LAG}$	1	-	-	us	From Last SCLK rising to NCS rising
NCS min. High Time	t_{NCS-HI}	2	-	-	us	From previous NCS rising to next NCS falling
SDIO Write Setup Time	$t_{SETUP-WR}$	250	-	-	ns	SDIO data valid before SCLK rising
SDIO Write Hold Time	$t_{HOLD-WR}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO delay after SCLK	t_{DLY-RD}	-	-	50	ns	From SCLK falling to SDIO data valid, no load conditions
SCLK delay for Data Preparation	$T_{PREP-RD}$	250	-	-	ns	The min. time between the falling of 8th SCLK and the rising of 9th SCLK
SDIO Read Hold Time	$t_{HOLD-RD}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO Rise Time	t_{SDIO-R}	-	30	-	ns	@C_L = 30 pF
SDIO Fall Time	t_{SDIO-F}	-	30	-	ns	@C_L = 30 pF
NCS min. High Time after QB pulse finished.	$t_{QB\_NCS\_LOW}$	500	-	-	ns	From previous QB falling to next NCS falling.

7.0 Hardware Pin Functions

7.1 MOTION Pin

Whenever the chip detects the occurrence of motion, the MOTION pin goes from high to low. The detected motion data (X-movement and Y-movement) is accumulated and stored in chip's internal buffer. The host controller can read out this motion data through register Delta_X (address 0x03 and 0x011) and Delta_Y(address 0x04 and 0x12). Before reading the motion data through the registers, be sure to read register Motion_Status (address 0x02) first to check if the Motion bit (bit 7) is 1. If the Motion bit is 1, the data in register Delta_X and Delta_Y is valid, otherwise it is invalid. The MOTION pin can also be used to monitor whether if the motion data stored in chip's internal buffer has been cleared (zero value). If the motion data is not cleared, the MOTION pin remains low. After all the motion data in chip's internal buffer is cleared, the MOTION pin goes high.

When the system is working at an idle state where the chip is at Sleep1/Sleep2/Sleep3 mode and the host controller is at idle mode, and when the chip detects the occurrence of motion, the MOTION pin goes low. This event on MOTION pin can be used as an interrupt event to wake up the host controller.

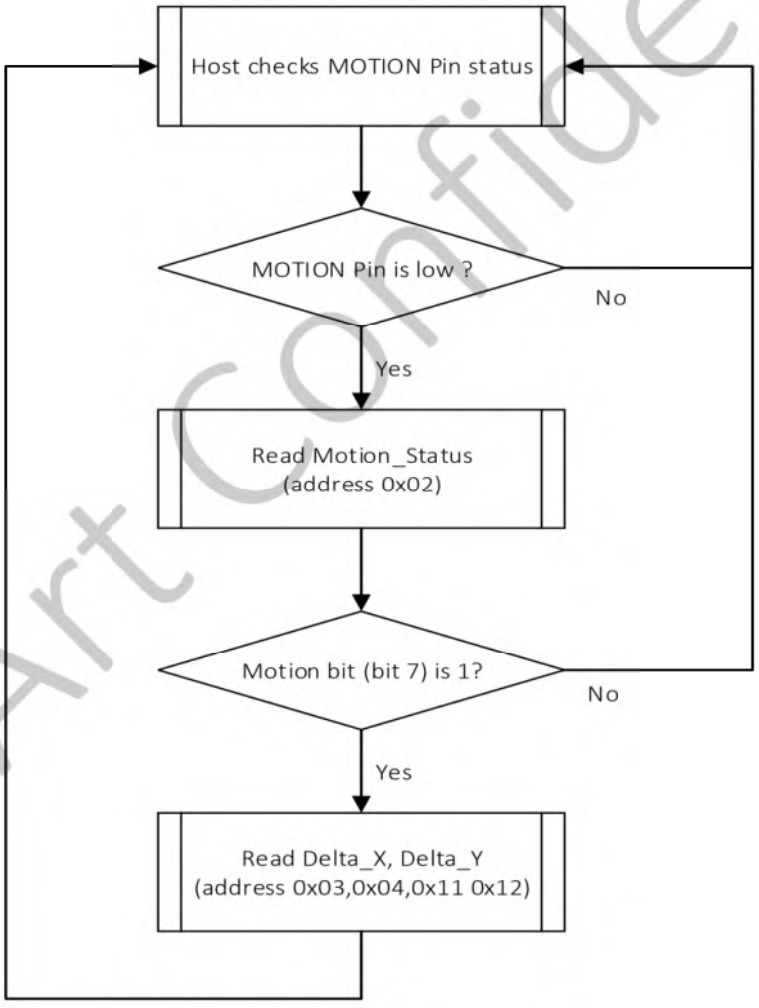
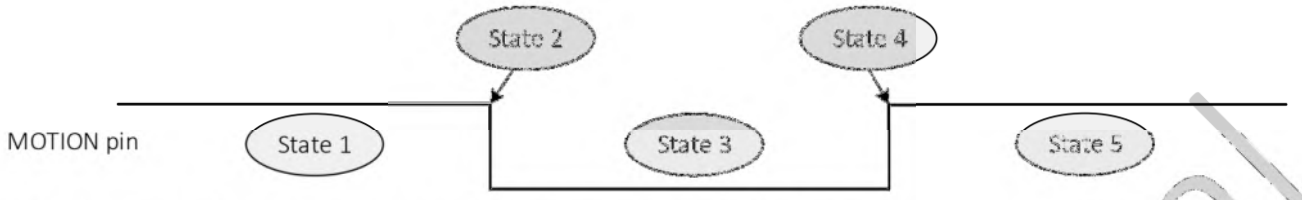


Figure 17. Motion Pin Flow Chart



State 1 : No motion detected. Register Motion bit =0, Delta_X and Delta_Y are invalid.
State 2 : Motion detected. Register Motion bit =1 and Delta_X and Delta_Y are valid to read (non-zero values).
State 3 : Motion continues. Register Motion bit =1 and Delta_X and Delta_Y are valid to read (non-zero values).
State 4 : Motion stops and the last reports of motion have been read out. Register Motion bit =0, Delta_X and Delta_Y are all inval
State 5 : No motion detected. Register Motion bit = 0, Delta_X and Delta_Y are invalid.

Figure 18. Motion Pin Waveform

7.2 Selection of MFIO Pin Functions

MFIO pin is a multi-functional input pin to be programmed through SPI interface for one the following four functions.

- Hardware Reset
- Quick-Burst
- Hardware Power-Down
- Null function (Default power-up setting)

- The function setting can be done via Bit[5:3] of register MFIO_Config (address 0x26) as below.
- 3'b000: Hardware Reset
- 3'b011: Quick-Burst
- 3'b100: Hardware Power-Down
- 3'b110: Null function

7.2.1 Hardware Reset (RST)

By pulling this RST pin to voltage high, a full chip reset will thus be executed and all the register values will be reset to the power-up default values. After the hardware reset was executed, the recommended register settings must be reloaded to ensure the chip is working properly.

7.2.2 Quick-Burst (QB)

The QB function is a quick method to dump out the motion data via SPI interface. As shown in Figure 19, by using this method the controller could save serial port accessing time up to 60% as compared to conventional read access. The minimum QB high pulse time to be asserted is 2µs.

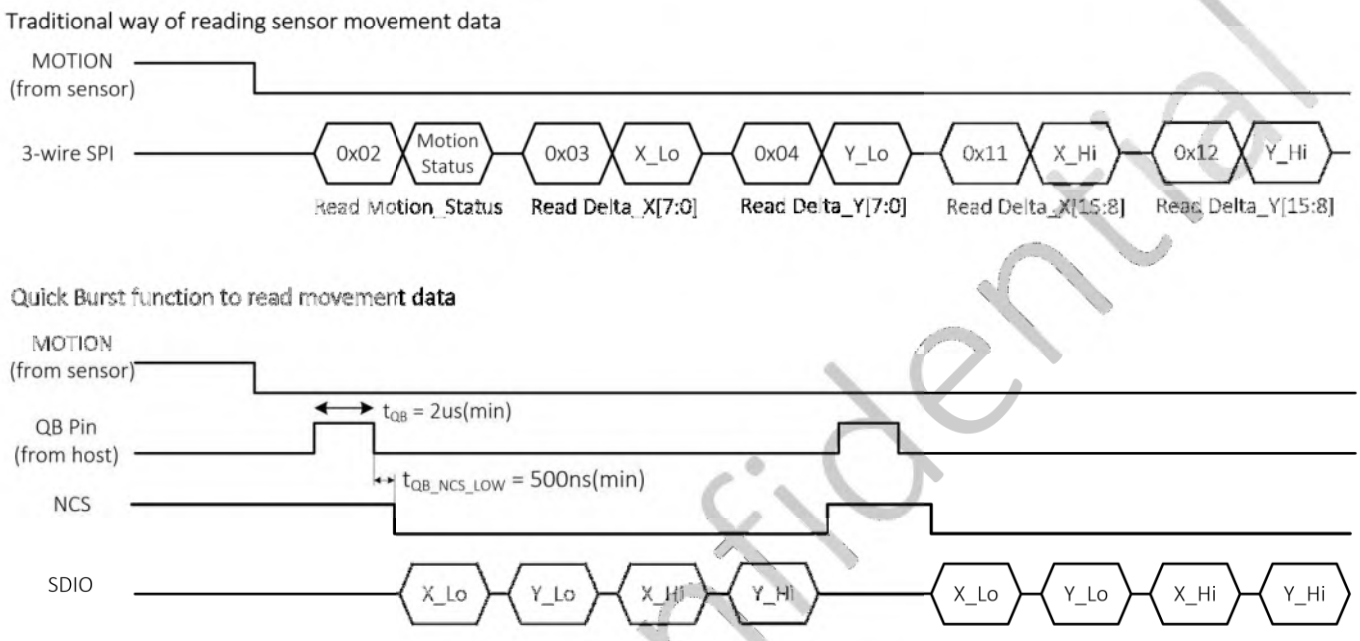


Figure 19. Quick Burst Function in SPI mode

7.2.3 Hardware Power-Down (PD)

By pulling PD pin to voltage high, the chip can enter into most low power saving state. In this state, all the chip register settings are retained and can be accessed through SPI interface as well. To get the chip out of this state, releasing MFIO pin to voltage low will do so. For more accurate motion reports, it is recommended that the host controller should wait at least 3ms before reading any motion reports after reset the MFIO pin to voltage low.

7.2.4 Null Function (NF)

When MFIO pin is programmed as NF mode, the chip will not have any response whenever MFIO pin is at high or low voltage.

8.0 Software Control Functions

8.1 Software Power-Down

The chip can also be put into the lowest power state in power-down mode by setting PD_EnH bit (Bit 3) in the Configuration register (address 0x06) through SPI interface. In power-down mode, all the chip register settings are retained and can be accessed through SPI interface as well. Reset PD_EnH bit will get the chip out of the power-down mode. To obtain correct motion data, it is recommended that the host controller should wait at least 3ms before reading the motion data after resetting the PD_EnH bit.

8.2 Software Reset

During power-up, the chip does not need an external power-on reset as there is an internal circuitry that performs power-on reset function in the chip. However the chip can also be soft reset by setting the Reset bit (Bit 7) of Configuration register (address 0x06). A full chip reset will thus be executed and then all the recommended register settings must be reloaded.

8.3 LED Current Source Control

An ideal way to control the LED current (I_{LED}) is to use the built-in programmable LED current source as shown in Figure 20. The chip internally generates the drive current (I_{LED}) for the integrated LED in pulsed mode. With the regulation of the current source circuitry, I_{LED} can keep its stability to offset the variation in VLED and the also variation in LED forward voltage (V_F) across different LED bin grades. The register LED_Current (address 0x51) provides the LED current source configuration.

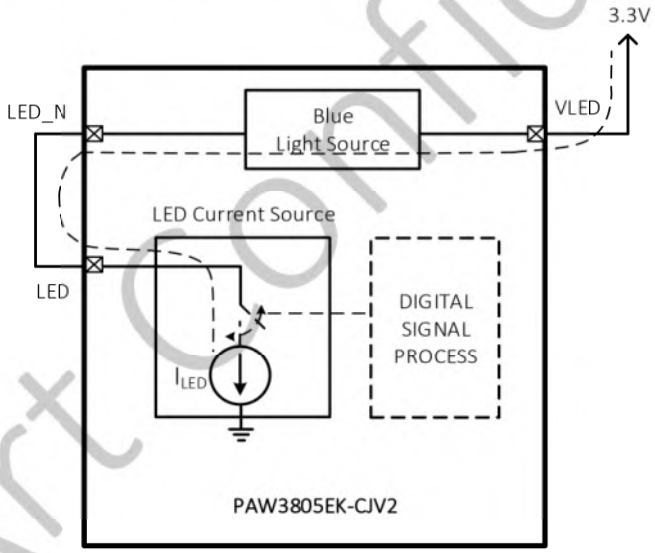


Figure 20. LED Current Source

Document Revision History

Revision Number	Date	Description
0.1	06 Dec 2016	New creation
1.0	30 Dec 2016	1. Added PCB cutout and footprints drawings in Section 3.1
1.1	17 Mar 2017	1. Modified the description in Section 7.2 2. Modified the description in register MFIO_Config (address 0x26) 3. Added $t_{OB\_NCS\_LOW}$ spec. in Figure 19 and Table 6 4. Modified the dimensions in Figure 3
1.2	05 Apr 2017	1. Modified Figure 1 and Figure 20