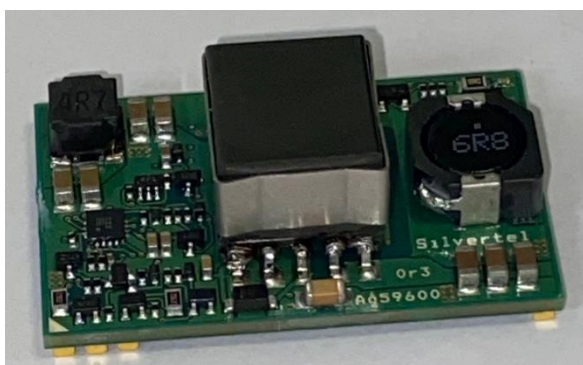




# Ag59600LPB

## Miniaturised Surface Mount 51W Power-over-Ethernet Module



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Zertifiziert nach ISO 9001:2015

## Description

The Ag59600LPB series Power-over-Ethernet (PoE++) modules are designed to extract power from a conventional twisted pair Category 5 Ethernet cable, conforming to the IEEE802.3 PoE standard, with full compatibility with the IEEE802.3bt, IEEE802.3at and IEEE802.3af amendments.

The Ag59600LPB is pre-configured as a Type 3 Class 6 device, requesting 60W of power from the PSE, with nominal output voltages of 12V or 24V.

The high efficiency DC/DC converter can achieve greater than 94% efficiency and operates over a wide input voltage range with a low ripple and low noise output. The DC/DC converter also has built-in output overload, output short-circuit and over-temperature protection and provides a 1500Vdc (input to output) isolation barrier.

## Features

- 51W power class PD, 60W peak output power (IEEE802.3bt)
- 94% efficient DC/DC converter
- 12V and 24V variants available
- Low output ripple & noise
- Overload, short-circuit and thermal protection
- Adjustable output voltage
- Industrial temperature range
- Minimal external components required
- Class 6 IEEE802.3 PD
- IEEE802.3bt, IEEE802.3at, IEEE802.3af compliant
- Small Surface mount (SMT) package size 44mm x 25mm x 16mm
- 1500Vdc isolation (input to output)
- Silvertel “design-in” assistance

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## 1 Product Overview

### 1.1 Ag59600LPB Product Selector

Part Number <sup>1</sup>	Nominal Output Voltage	Output Power	Marking <sup>2</sup>	Package
Ag59612LPB	12V	51W <sup>3</sup> Continuous, 60W Peak	ab12c	SMT
Ag59624LPB	24V		ab24c	

Note 1: Complies with the European Directive 2011/65/EU for the Restriction of use of certain Hazardous Substances (RoHS) including Directive 2015/863 published in 2015, amending Annex II of Directive 2011/65/EU. Moisture Sensitive Level 1 and HBM 1.

Note 2: Located on the transformer.

The first letter, a, indicates the week as A-Z with uppercase being weeks 1-26, lower case weeks 27-52.

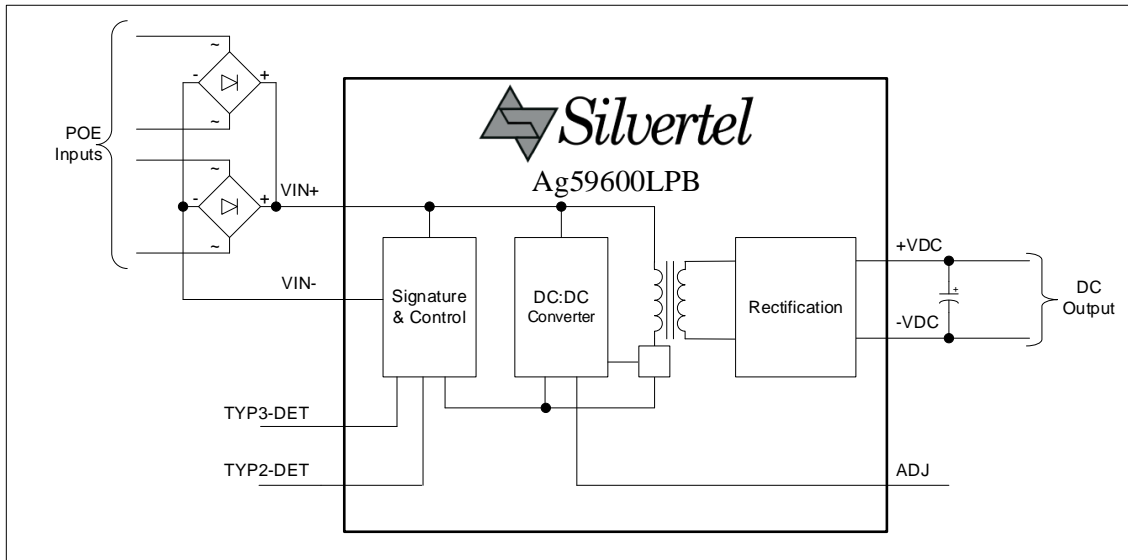
The second letter, b, indicates the year in uppercase A-Z starting from 2020.

The two digits are the nominal output voltage,

The final letter, c, is a Silvertel reference.

Note 3: Limited by PSE output power and transmission losses

**Table 1: Ordering Information**



**Figure 1: Block Diagram**

## 1.2 Package Format

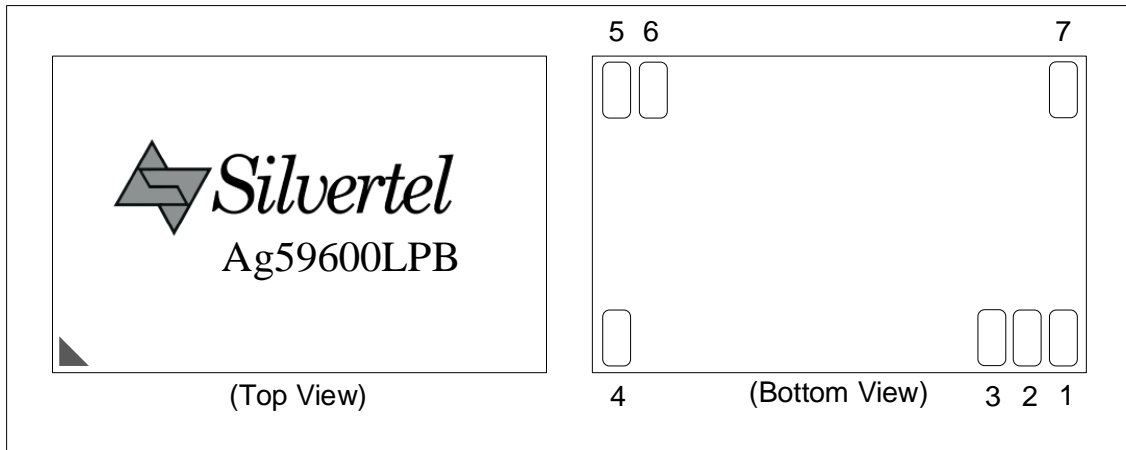


Figure 2: Ag59600LPB Package Format

## 1.3 Pin Description

Pin #	Name	Description
1	$V_{IN-}$	<b>POE Direct Input -.</b> This pin connects to the negative (-) output of the POE input bridge rectifiers.
2	TYP2-DET	<b>Type 2 Detect Output.</b> This pin indicates if an IEEE802.3at PSE is supplying power to the Ag59600LPB; see Section 1.5.3 for more details.
3	TYP3-DET	<b>Type 3 Detect Output.</b> This pin indicates if a IEEE802.3bt Type 3 or Type 4 PSE is supplying power to the Ag59600LPB; see Section 1.5.3 for more details.
4	$V_{OUT+}$	<b>Positive DC Output.</b> This pin provides the positive regulated output from the Ag59600LPB.
5	$V_{OUT-}$	<b>Negative DC Output.</b> This pin provides the negative regulated output from the Ag59600LPB.
6	ADJ	<b>Output Adjust.</b> The output voltage can be adjusted from its nominal value, by connecting an external resistor from this pin to either the +VDC pin or the -VDC pin.
7	$V_{IN+}$	<b>POE Direct Input +.</b> This pin connects to the positive (+) output of the POE input bridge rectifiers.

Table 2: Pin Description

### 1.4 Typical Connections

The Ag59600LPB only requires a few external components - the bridge rectifiers on the  $V_{IN}$  input are to conform to the input polarity protection requirement. The  $1000\mu\text{F}$  capacitor (C1) connected across the output is required for correct operation of the DC/DC converter. This capacitor must be positioned as close to the output pins as possible for optimal stability. It can be a low-cost electrolytic capacitor as shown in Figure 3; it does not need to be a low ESR type for operation in temperatures down to  $0^{\circ}\text{C}$ . But if ambient temperatures below  $0^{\circ}\text{C}$  are expected, a capacitor that retains a moderately low ESR and the minimum capacitance is essential for operation. Polymer Aluminium Solid Electrolytic Capacitors are ideal for this application.

The output voltage can be adjusted by simply connecting a resistor between the ADJ pin and either the +VDC Pin or the -VDC pin, see section 1.6.2 Output Voltage Adjust Setting.

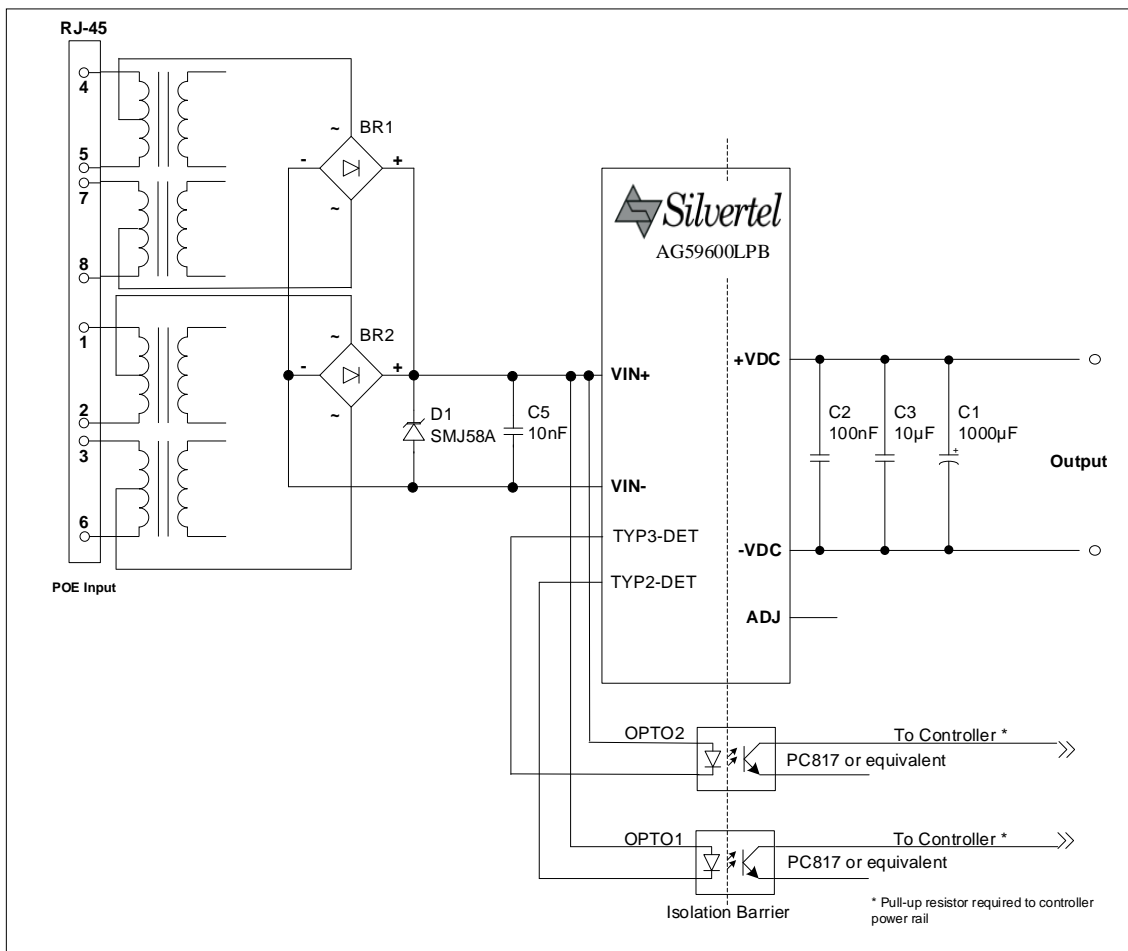


Figure 3: Typical System Diagram

## 1.5 Input

The Ag59600LPB has two input pins VIN+ and VIN-, these pins should be connected to the outputs of two external bridge rectifiers (see Figure 3: Typical System Diagram). This allows the Ag59600LPB to be compatible with Power Sourcing Equipment (PSE) that utilise any of the different power polarities permissible

The Ag59600LPB is designed to be powered by any compliant IEEE802.3 PSE such as Silvertel's Ag6800.

### 1.5.1 PD Signature

The Ag59600LPB complies with the IEEE802.3 specifications and provides signature and control circuitry specified within. When the inputs are connected to a PSE, they will automatically present a Powered Device (PD) signature to the PSE (when requested). The equipment will then recognise that a PD is connected to that line and supply power.

### 1.5.2 Power Classification

The Ag59600LPB is a fixed Type 3 - Class 6 PD requesting 60W of power from a compliant IEEE802.3 Type 3 or greater PSE by displaying the correct class pulses shown in Table 3 below. If the Ag59600LPB is connected to a Type 1 or Type 2 PSE, the PSE will recognise the Class request as a valid request beyond maximum output and default to its highest output classification power level, and supply 15.4W for a type 1 PSE and 30W for a Type 2 PSE.

Requested Class	Class Pulse Count	Pulse 1&2 Classification Current (mA)	Pulse 3+ Classification Current (mA)	PSE Output Power (W)	Min. Available PD Power (W)	IEEE Spec. Amendment
0	1	<5	N/A	15.4	12.75	802.3af
1	1	10	N/A	4	3.84	
2	1	20	N/A	7	6.49	
3	1	30	N/A	15.4	12.75	
4	2 or 3	40	40	30	25.5	802.3at
5	4	40	<5	45	40	802.3bt
6	4	40	10	60	51	
7	5	40	20	75	62	
8	5	40	30	90	71.3	

**Table 3: Classification Table**

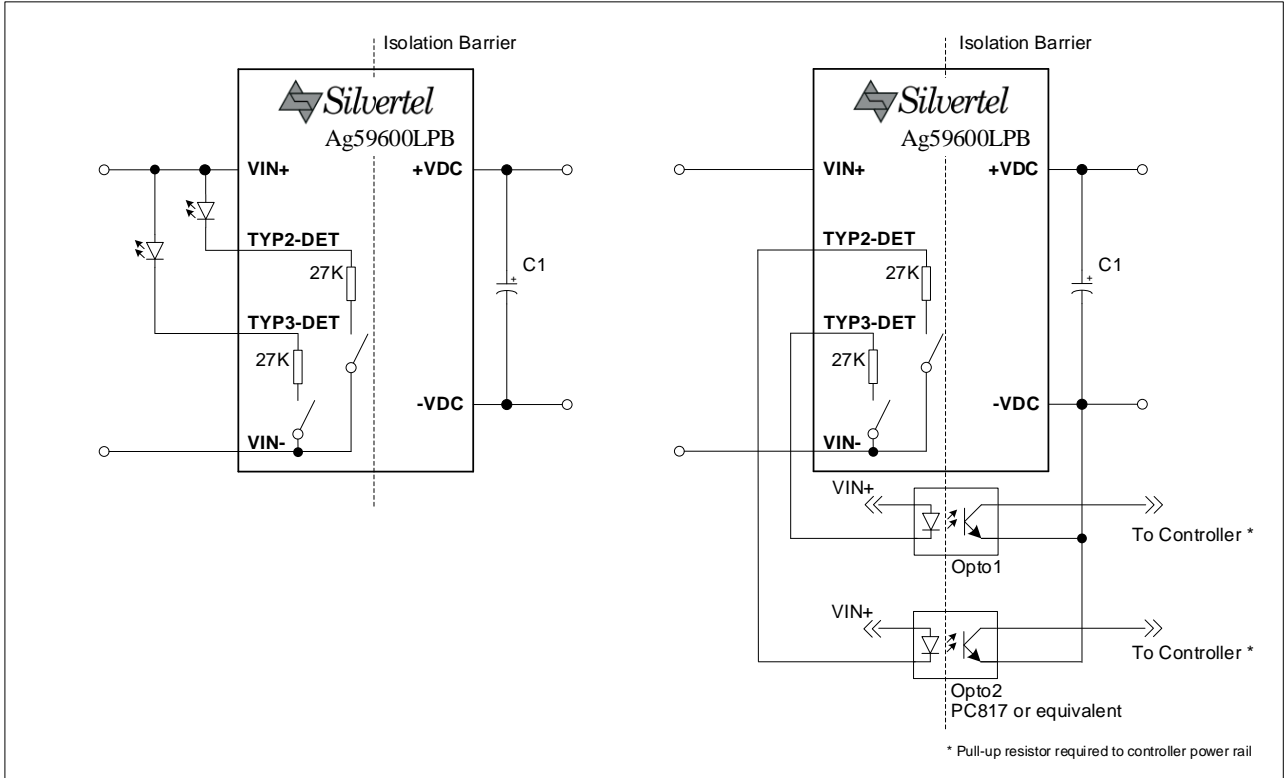
### 1.5.3 PSE Type Detection

The IEEE802.3 specification stipulates that if a device detects it is connected to a PSE that is not capable of providing the full requested power level, the device should either remain in a reduced power mode and indicate to the user that the device is under powered.

To achieve this, the Ag59600LPB monitors the detection and classification sequence to determine the type of PSE that performed the signature and classification. The module uses the two type detection output pins, TYP2-DET and TYP3-DET, to flag to either the application circuitry or the user the detected PSE type to either adjust the peak power

draw of the application or to inform the user that the device is under powered and may power cycle.

When the PSE type has been detected, the relevant pin will pull low from Vin+ this can be used to drive an LED or an Optocoupler as shown in Figure 4.



**Figure 4: Physical Layer Detect Configuration.**

If the Ag59600LPB detects a greater than three Event Physical Layer classification, the switch will close and Opto2 will turn ON and Opto1 will be OFF. Opto2 will pass this signal across the isolation barrier and the output collector can be connected to a controller (with a pull-up resistor connected to the controller’s power rail). When Opto2 is ON the collector (output) will be Logic 0, the controller will then know that the PSE is capable of delivering 60W. To complete the protocol (and conform to the IEEE802.3 specification) the controller should then confirm that it is a Type 3 PD over the Data Link Layer\*.

If the Ag59600LPB detects a Single Event Physical Layer classification, both Opto1 and Opto2 will be OFF and the output collectors will be Logic 1 (via pull-up resistor). The controller should then assume that the PSE is limited to only delivering up to 15.4W. If the Ag59600LPB detects a Two Event Physical Layer classification, Opto1 will be ON and Opto2 will be OFF. The controller should then assume that the PSE is limited to only delivering up to 30W.

If the PSE does not support the Physical Layer classification, Opto1 and Opto2 will be OFF.

The Ag59600LPB may operate with some PSEs that are not compliant to the IEEE802.3 specification.

\*There are several PSEs (including Cisco) that will only deliver  $\leq 15.4W$  until they receive confirmation over the Data Link Layer.

### 1.6 Output

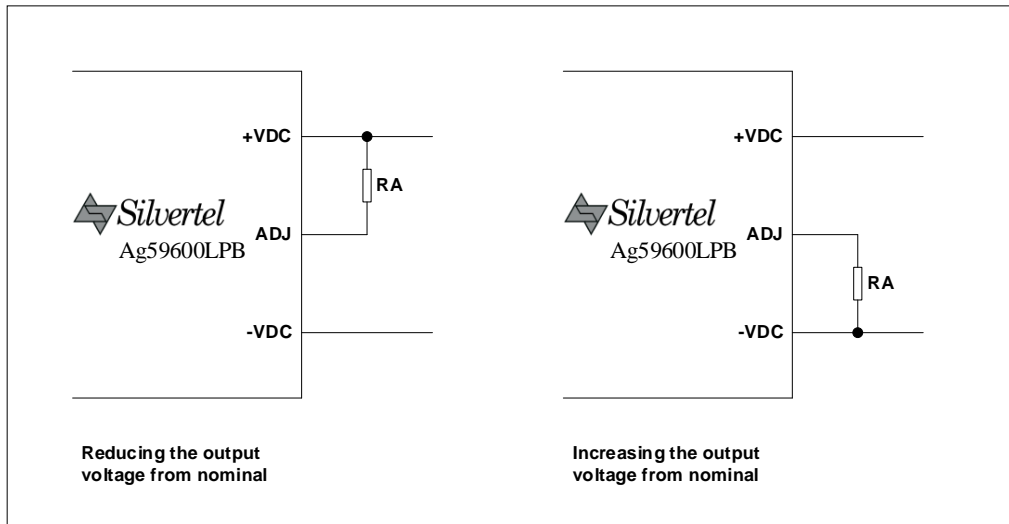
#### 1.6.1 Maximum output power

While the Ag59600LPB is capable of delivering a peak power output of 60W, this will be limited by the available delivered power at the input pins of the module. Due to system losses only 51W is guaranteed to the application device. As a result, any application should be design for a maximum continuous output power of 48W from the Ag59600LPB.

A Type 3 or greater (IEEE802.3bt) PSE supplying Class 6 power levels shall provide a minimum of 60W at its lowest voltage of 52V from its output, however with cable, connector and rectification losses, the available power and voltage at the input pins of the Ag59600LPB may vary considerably. In a fully compliant IEEE802.3 system, the power available, measured at the input to the bridge rectifiers, may be as low as 51W. See “ANX-POE-Power” for more details.

#### 1.6.2 Output Voltage Adjust Setting

The Ag59600LPB has an output voltage adjustment pin, ADJ, which can be used to either increase or decrease the output voltage of the module.



**Figure 5: Output Voltage Adjustment**

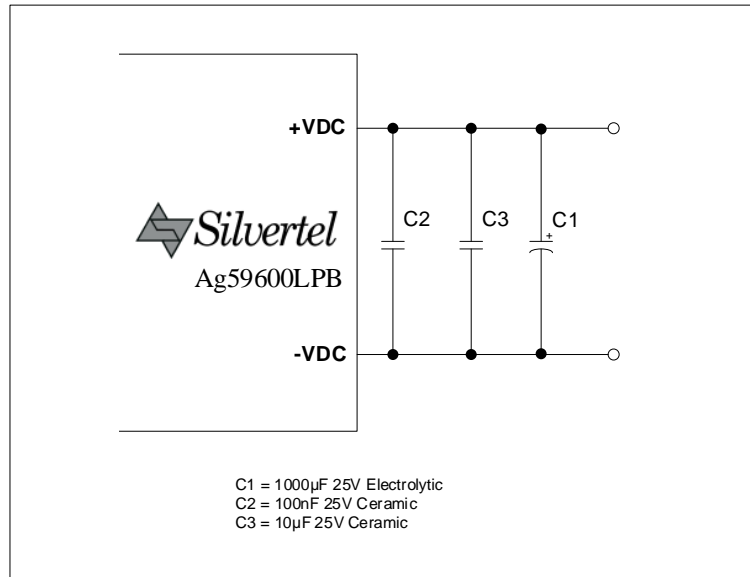
Reducing the output voltage, connect RA between ADJ and +VDC		
Value of RA	Ag59612LPB output	Ag59624LPB output
Open Circuit	12.0V	24.0V
0 Ohms	8.8V	18.9V
Increasing the output voltage, connect RA between ADJ and -VDC		
Value of RA	Ag59612LPB output	Ag59624LPB output
Open Circuit	12.0V	24.0V
0 Ohms	13.2V	25.0

**Table 4: Output Voltage Adjustment Resistor Values**



### 1.6.3 Output Filtering

The Ag59600LPB requires a bulk capacitance to be fitted on its output for stable operation, this is typically provided with just an electrolytic capacitor, this provides a high level of output regulation and low output ripple. The recommended output filtering is shown in Figure 6.



**Figure 6: Output Filter**

## 2 Operating Temperature Range

At the heart of the Ag59600LPB is a DC/DC converter, it will generate heat. While the product has been designed to be a high efficiency device, the small form factor requires that thermal management is taken into consideration at the design stage. The amount of heat generated by the module will depend on the load it is required to drive and the input voltage supplied by the PSE.

The Ag59600LPB can operate up to a maximum of 85°C ambient, and a minimum of -40°C ambient. When intended for used in ambient temperatures below 0°C it is recommended that an output capacitor that will retain the minimum output capacitance and ESR ratings for the Ag59600LPB at the lowest temperature in the intended operating range is used. A Polymer Aluminium Electrolytic Capacitor is ideal for this application, however a reputable brand rated to -55°C should suffice for most applications, please contact Silvertel if suggestions are required.

## 2.1 Thermal Considerations

Each application is different; therefore, it is impossible to give fixed and absolute thermal recommendations. Due to the miniaturised design, while not required, it is recommended that a thermal interface material is used between the module and the host PCB to draw heat out and away from the module for continuous operation. It is recommended to make provision for heatsinking as follows.

The recommended method for drawing heat away from the Ag59600LPB is by means of copper planes connected to the power pins of the Ag59600LPB along with a thermal gap filler gel fitted underneath the Ag59600LPB, such as Parker Chomerics THERM-A-GAP GEL. This technique can be used to draw heat away from the DC/DC converter to dissipate over a larger surface area.

The copper planes should be on the outer layers of the PCB, best results are achieved with additional copper planes on internal layers of host PCB with multiple thermal via connections. An example of this is shown in Figure 7. It is also important that any enclosure has sufficient ventilation for the Ag59600LPB.

It is recommended that the gap filler is applied to this region such that it encompasses both the components and PCB. The gap filler can be used in combination with thermal via arrays, to reduce the thermal resistance between the copper planes. Figure 8 shows the recommended application area for the gap filler to provide sufficient heat transfer from the module to the host PCB.

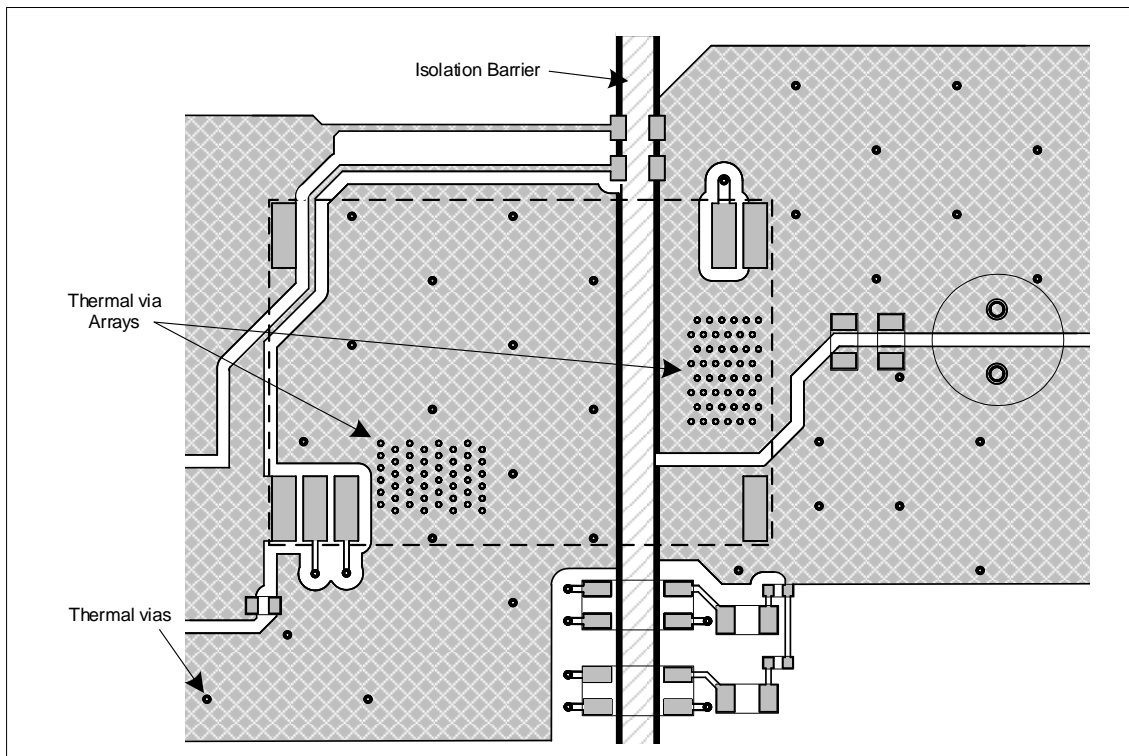
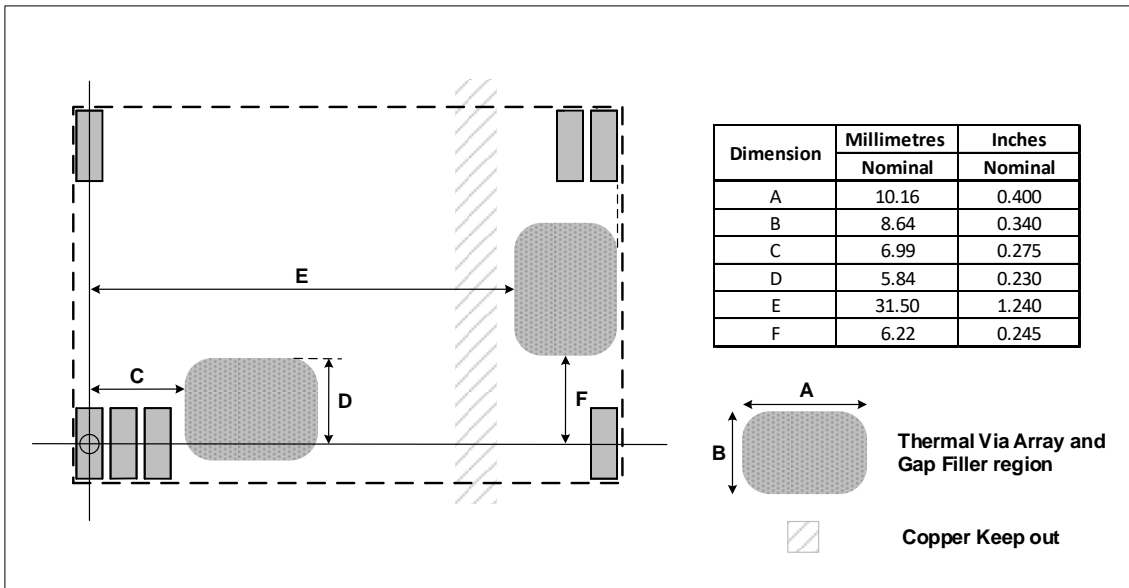
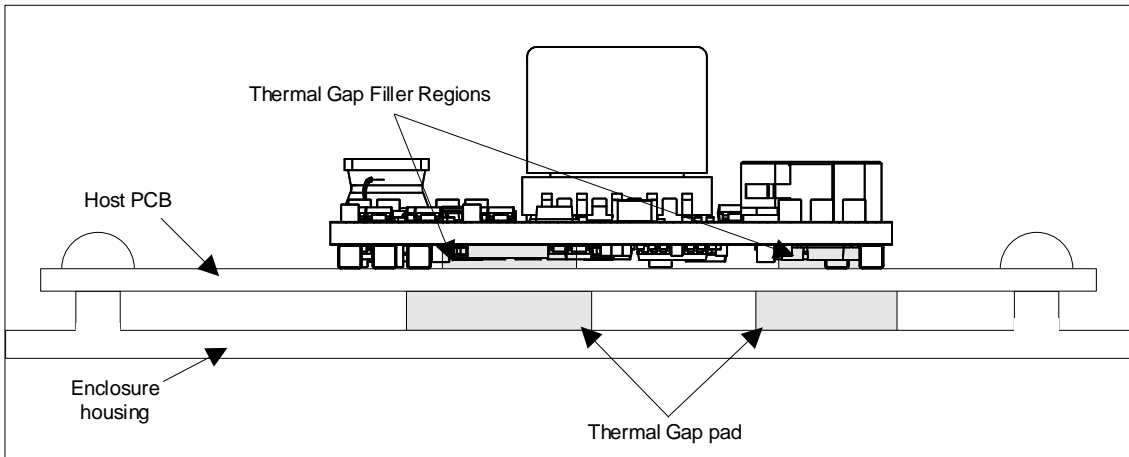


Figure 7: Thermal Relief



**Figure 8: Thermal Interface Application Region**

Heat dissipation can be improved further by thermally connecting to the enclosure of the application. The simplest method of performing this is to use a thermal gap pad located between the host PCB and the enclosure, situated over the area containing the thermal via arrays.



**Figure 9: Additional Heatsinking**

## 3 Protection

### 3.1 Input Protection

The Ag59600LPB will shut down the DC/DC converter if a voltage exceeding the maximum supply rating is detected.

The Ag59600LPB may be damaged by input voltage transients greater than 80V, while the module contains a TVS diode on board, removing the requirement for fitting external protection in the vast majority of applications. If additional protection from electrostatic discharge (ESD) or other high voltage transients is required, an additional over-voltage clamping device can be fitted across the VIN+ and VIN- input pins, see Figure 10 and Apps Note “ANX-POE-Protection” for more details.

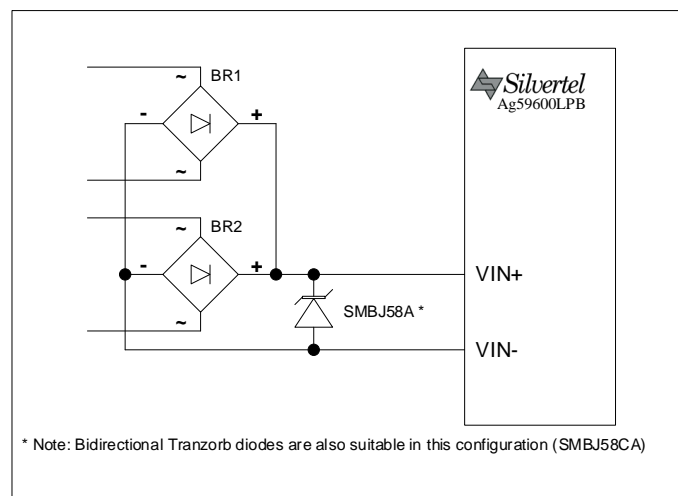


Figure 10: Input Protection

### 3.2 Output Back Feed Protection

If an external or auxiliary supply is to be used, it is essential that a blocking diode is present to prevent voltage injection on to the output circuitry of the module. This may cause damage to the module. The back feed protection is required even if the external voltage is present only while the module remains unpowered.

### 3.3 Output Short Circuit Protection

The Ag59600LPB has over-current protection to prevent the module from becoming damaged in the event of a short circuit event. If an over current event occurs the Ag59600LPB will disable the output, the Ag59600LPB will then test the current draw approximately every 2 seconds until the cause of the over current is removed, after which, the power will be restored to the output.

### 3.4 Thermal Protection

The Ag59600LPB contains built in thermal protection to prevent the module becoming damaged in the event that it is operated beyond its temperature specification. When the Ag59600LPB has detected it is over temperature, the output will be disabled until the module has cooled sufficiently.

## 4 Isolation

To meet the safety isolation requirements of IEEE802.3 specification, a powered device must provide electrical isolation between all its accessible external connectors, including frame ground. In order to meet this requirement, the powered device should be subjected to and pass at least one of the following electrical strength tests of IEC 60950-1:2001 sub clause 6.2.1.

- a) 1500V<sub>rms</sub> at 50-60Hz for 60 seconds
- b) 2250V<sub>dc</sub> for 60 seconds or
- c) 1500V<sub>dc</sub> impulse test 10 times in either polarity.

To assist in this the Ag59600LPB has been designed to meet and pass the 1500V<sub>dc</sub> impulse test with no breakdown of insulation.

In order to maintain this isolation requirement, it is essential that that the isolation barrier is not breached, see ANX-POE-Isolation-Barrier for more details.

## 5 EMC

The Ag59600LPB has been designed to pass EN55032 Class B, however the Ag59600LPB will only be one component within the system so we would always advise that provisions are put in place in case further noise reductions are needed. From our experience we would recommend an inexpensive but effective solution to reduce emissions as shown in Figure 11, for more details please see ANX-POE-EMI-Considerations.

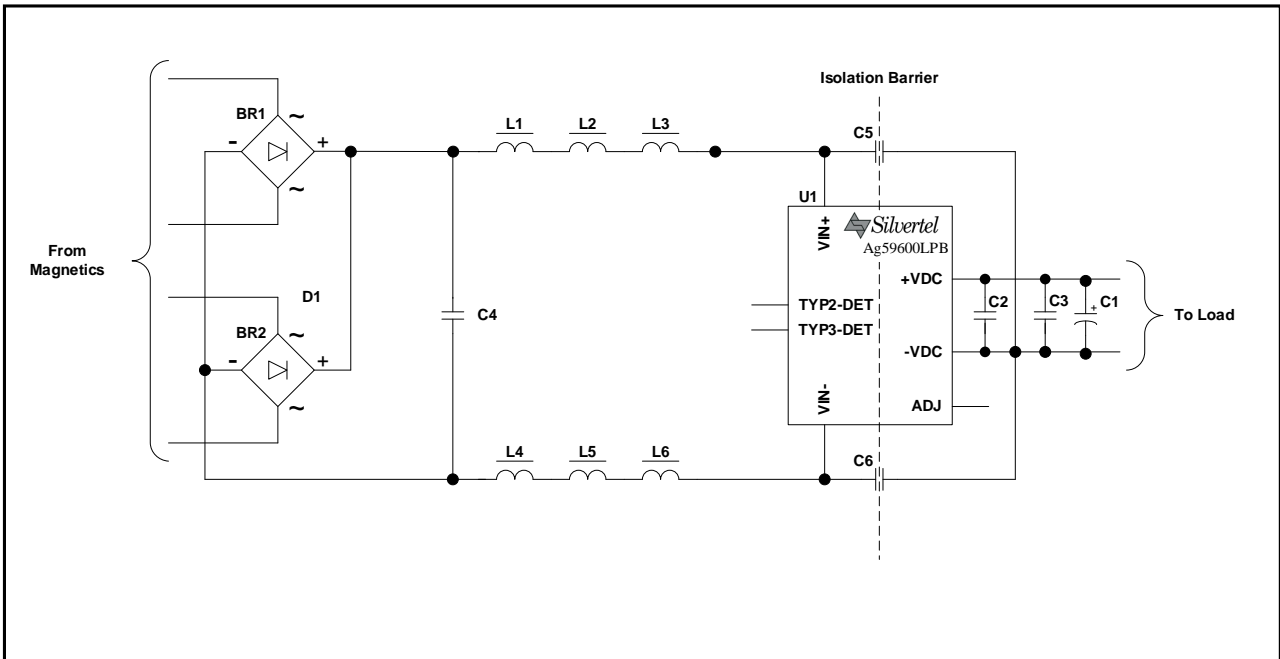


Figure 11: Typical Connection Diagram

## 6 Solderability

The Ag59600LPB has been designed with a fully automated assembly process in mind and is lead-free (Pb-free) and RoHS compliant and fully compatible with a Pb-free automated assembly process. The Ag59600LPB can still be mounted manually using soldering iron or hot air.

There are no specific requirements regarding stencil thickness or solder paste classification type. Solder mask defined (SMD) pads are preferred over non-solder mask defined (NSMD) pads, the land pattern dimensions are given in Figure 13.

Minimal thermal relief should be applied to the pads to allow for maximum thermal conductivity without hindering the reflow process, your Process Engineer should be able to provide suitable recommendations.

The Ag59600LPB requires no components of greater than Moisture Sensitivity level 1, as a result no special processes are required in the reflowing process of the Ag59600LPB.

Note : Do not pass the Ag59600LPB through the reflow process mounted to the underside of the assembly due to the risk of components falling off the module.

### 6.1 Solder Profile

Below is a typical profile that the Ag59600LPB should be mounted, based on the J-STD-020 standard for Pb-Free applications. Exceeding these specifications may cause damage to the module. All production environments are different therefore please review these guidelines with the process engineer prior to use.

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Units
Zone Duration	42	42	42	42	42	Seconds
Top Heater	150	180	210	240	270	°C
Bottom Heater	150	180	210	240	270	°C
Typical Slope	2.1	1.2	1.1	0.9	0.8	°C/Second
Airflow rate	40					M <sup>3</sup> /Minute

**Table 5: Solder Profile**

	Min	Max	Units
Soak Time (s) 150-180°C	30	90	Seconds
Time above (s) ≥220°C	30	90	Seconds
Peak Temperature (°C)	230	255	°C
ΔTemperature (°C/s)	-3	3	°C/Second

**Table 6: Solder Parameters**

## 7 Electrical Characteristics

### 7.1 Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltage	V <sub>CC</sub>	-0.3	60	V
2	Storage Temperature	T <sub>S</sub>	-40	+100	°C
3	Moisture Sensitivity Level	MSL	-	1	-

Note : Exceeding the above ratings may cause permanent damage to the product. Functional operation under these conditions is not implied. Maximum ratings assume free airflow.

### 7.2 Recommended Operating Conditions

	Parameter	Symbol	Min	Typ	Max	Units	
1	Input Supply Voltage	V <sub>IN</sub>	41 <sup>1</sup>	54	57	V	
2	Transient Supply Voltage <sup>1</sup>	V <sub>TRAN</sub>	36			V	
3	Input Under Voltage Lockout	V <sub>ULOCK</sub>		37		V	
4	Input Under Voltage Lockout	V <sub>ULOCK-Hsy</sub>		2.5		V	
5	Operating Temperature	T <sub>OP</sub>	-40	25	85	Ta / °C	
6	Output capacitance	Ag59612LPB	C <sub>out</sub>	470	1000	1500	μF
		Ag59624LPB		330	470	680	

Note 1: At ≤ 50% load

### 7.3 DC Electrical Characteristics

	DC Characteristic		Sym	Min	Typ <sup>1</sup>	Max	Units	Comments
1	Nominal Output Voltage	Ag59612LPB	+V <sub>OUT</sub>	11.5	12	12.5	V	
		Ag59624LPB		23.25	24	24.8		
2	Continuous Current output <sup>2</sup>	Ag59612LPB	I <sub>LOAD</sub>		4.25	4.5	A	
		Ag59624LPB			2.1	2.5		
3	Line Regulation		V <sub>LINE1</sub>		0.1		%	@ 50% load
4	Load Regulation		V <sub>LOAD1</sub>		0.5		%	@ 52V <sub>in</sub>
5	Ripple and Noise <sup>3</sup>	Ag59612LPB	V <sub>RN</sub>		68		mV <sub>p-p</sub>	At Full Load
		Ag59624LPB			TBC			
6	Minimum Load		I <sub>MIN</sub>	0			mA	
7	Short-Circuit Duration		T <sub>SC</sub>			∞	sec	
8	Peak Efficiency <sup>2</sup>	Ag59612LPB	EFF		94.1		%	
		Ag59624LPB			93.1			
9	Isolation Voltage (I/O)		V <sub>ISO</sub>			1500	V <sub>PK</sub>	Impulse Test

Note 1: Typical figures are at 25°C with a nominal output voltage with 57V supply with a 470µF output capacitor fitted and are for design aid only. Not Guaranteed.

Note 2: Minimum 44V<sub>in</sub> for maximum output at 25°C. Maximum output power may be limited by PSE.

Note 3: Measured with external filter A. The output ripple and noise can be reduced further with external filter B, see Section 1.6.3.



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### 8 Package

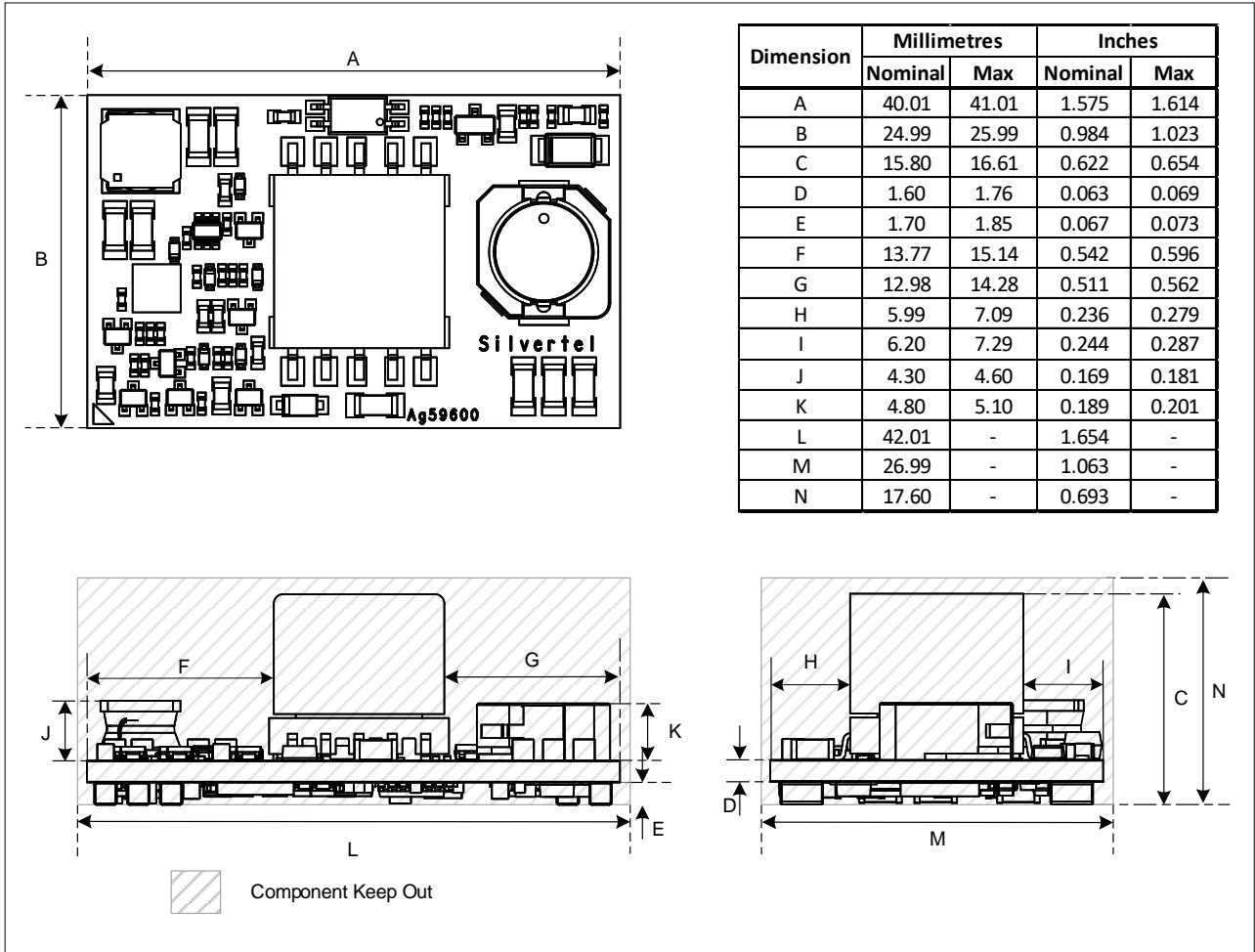


Figure 12: Package Dimensions

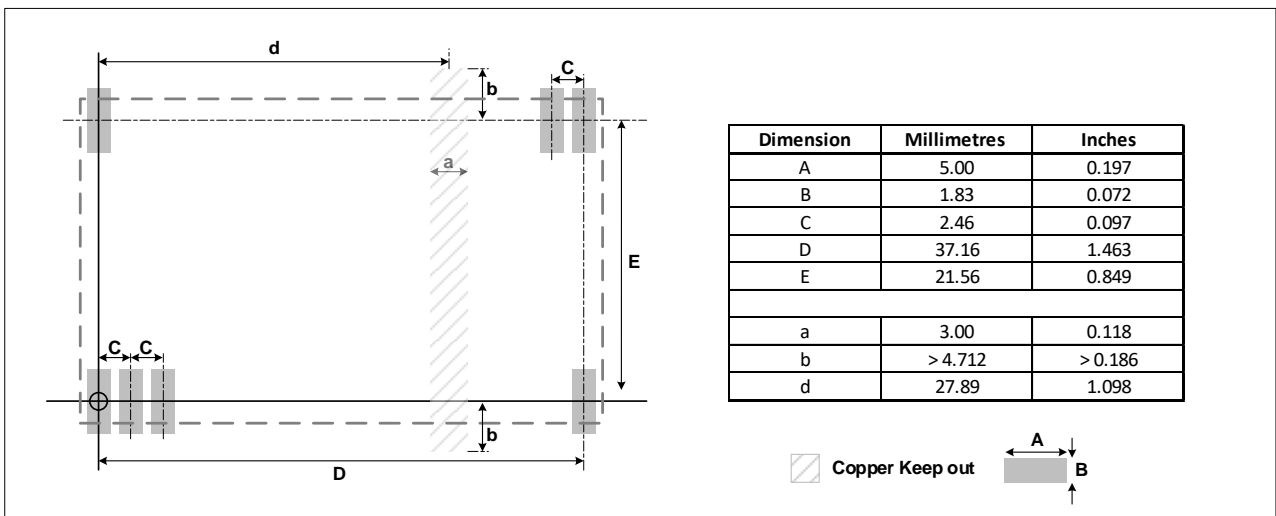


Figure 13: Land Pattern

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