

# INN040FQ015A

40V GaN Enhancement-mode Power Transistor

## INN040FQ015A

### 1. General Description

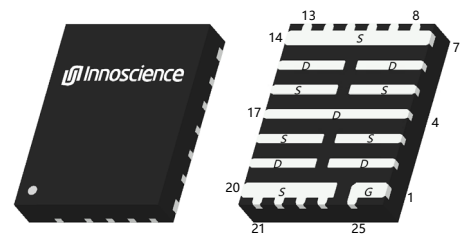
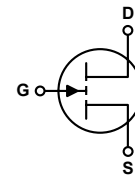
GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 5 mm x 4 mm package size.

### 2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Zero reverse recovery charge

### 3. Applications

- Battery Charger
- Battery Management System
- Notebook
- Industry



### 4. Key Performance Parameters

Table 1 Key performance parameters at  $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	40	V
$R_{DS(on),max}$ @ $V_{GS} = 5\text{ V}$	1.5	m $\Omega$
$Q_{G,typ}$ @ $V_{DS} = 20\text{ V}$	28	nC
$I_{DS,Pulse}$	200	A
$Q_{OSS}$ @ $V_{DS} = 20\text{ V}$	58	nC

### 5. Pin Information

Table 2 Pin information

Pin	Pin description	Pin function
1,25	Gate	Driver Gate
3,5,7-14,16,18,20-24	Source	Source
2,4,6,15,17,19	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN040FQ015A	FCQFN 5mm x 4mm	D15

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### 6. Maximum Ratings

at  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

**Table 4** Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	40	V
$I_D$	Continuous current	50	A
	Pulsed ( $25\text{ }^\circ\text{C}$ , $T_{Pulse} = 100\text{ }\mu\text{s}$ )	200	A
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	$^\circ\text{C}$

## 7. Thermal Characteristics

**Table 5 Thermal characteristics**

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12	°C/W	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>1</sup>	30.5	°C/W	
$T_{sold}$	Maximum reflow soldering temperature	260	°C	MSL3

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

### 8. Electric Characteristics

at  $T_j = 25\text{ }^\circ\text{C}$ , unless specified otherwise

**Table 6** Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$BV_{DSS}$	Drain-to-Source Voltage	40			V	$V_{GS} = 0\text{ V}$ , $I_D = 1.1\text{ mA}$
$I_{DSS}$	Drain Source Leakage		0.04	0.9	mA	$V_{GS} = 0\text{ V}$ , $V_{DS} = 32\text{ V}$
$I_{GSS}$	Gate-to-Source Forward Leakage		0.04	0.8	mA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage		0.04	0.4	mA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.7	1.1	2.3	V	$V_{DS} = V_{GS}$ , $I_D = 25\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance		1.2	1.5	m $\Omega$	$V_{GS} = 5\text{ V}$ , $I_D = 15\text{ A}$
$V_{SD}$	Source-Drain Forward Voltage		1.25		V	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$

**Table 7 Dynamic characteristics**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$C_{iss}$	Input Capacitance		3.5		nF	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$
$C_{oss}$	Output Capacitance		1.6			$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$
$C_{rss}$	Reverse Transfer Capacitance		0.1			$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$
$C_{oss(er)}$	Energy Related $C_{oss}$		2.5			$V_{DS} = 0\text{ V to } 20\text{ V}, V_{GS} = 0\text{ V}$
$C_{oss(tr)}$	Time Related $C_{oss}$		2.9			
$R_G$	Gate resistance		1.6		$\Omega$	$f = 5\text{ MHz}$
$Q_G$	Total Gate Charge		28		nC	$V_{GS} = 5\text{ V}, V_{DS} = 20\text{ V}, I_D = 15\text{ A}$
$Q_{GS}$	Gate to Source Charge		6.2			$V_{DS} = 20\text{ V}, I_D = 15\text{ A}$
$Q_{GD}$	Gate to Drain Charge		4.6			$V_{DS} = 20\text{ V}, I_D = 15\text{ A}$
$Q_{G(TH)}$	Gate Charge at Threshold		4.3			$V_{DS} = 20\text{ V}, I_D = 15\text{ A}$
$Q_{OSS}$	Output Charge		58			$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$

## 9. Electric Characteristics Diagrams

at  $T_j = 25\text{ }^\circ\text{C}$ , unless specified otherwise

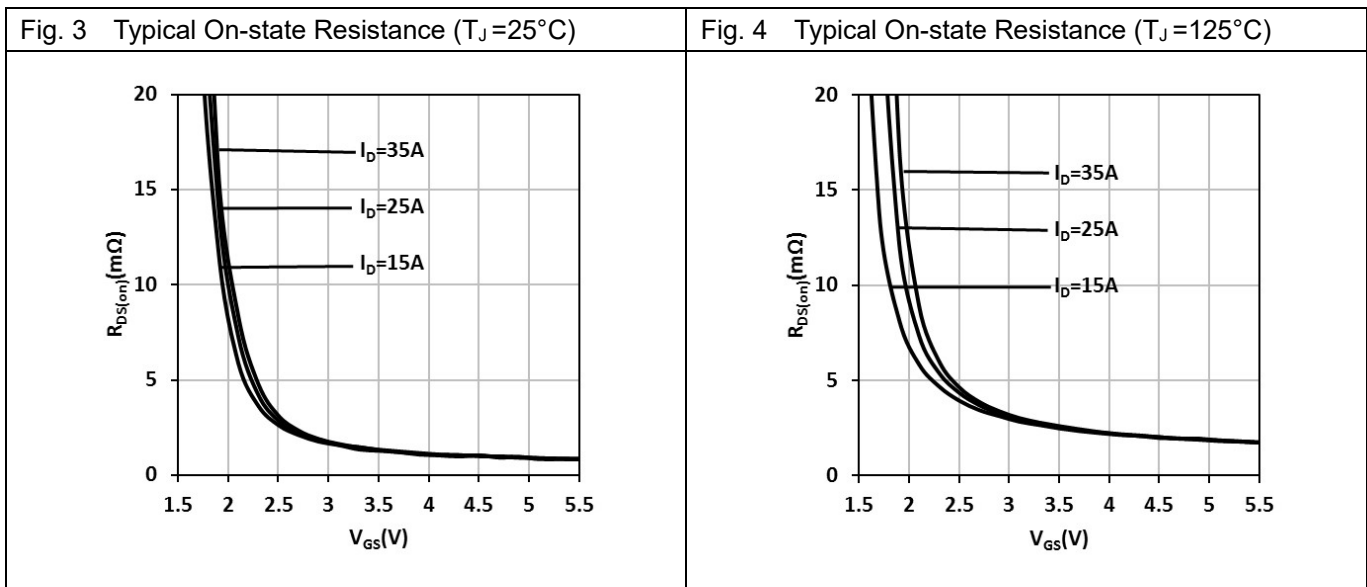
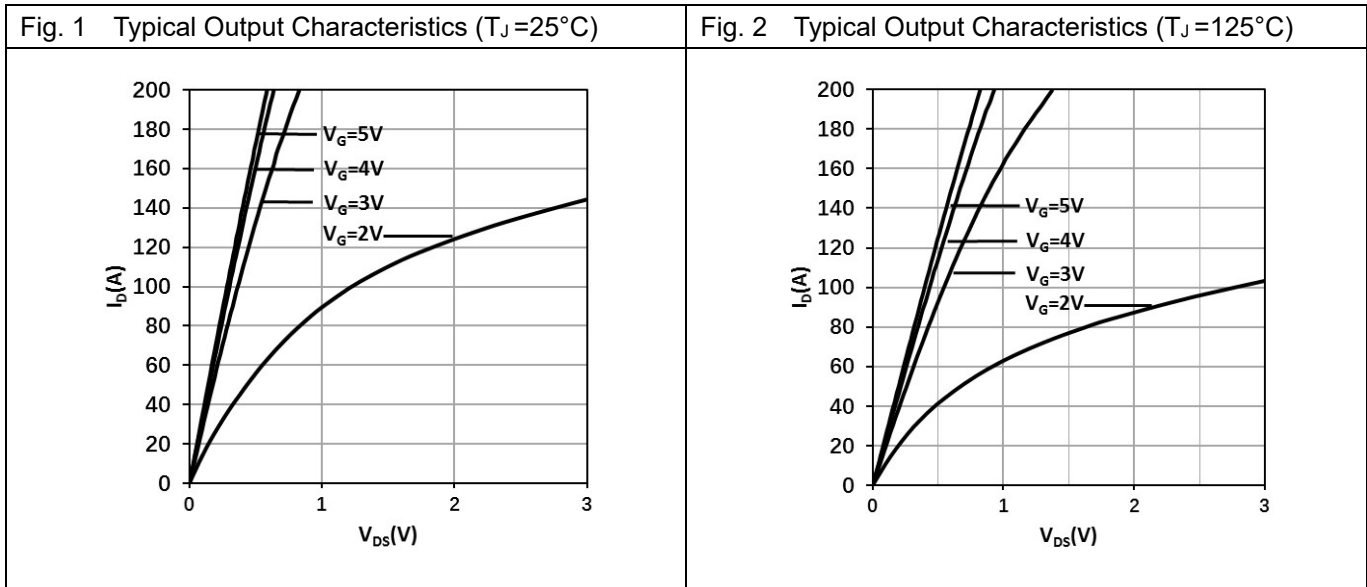


Fig. 5 Normalized On-State Resistance vs. Temp.

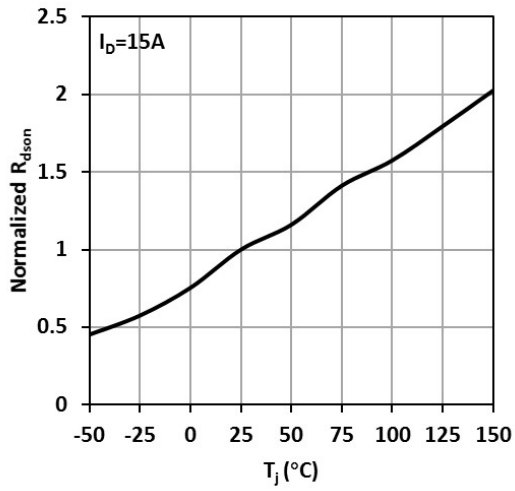


Fig. 6 Typical Transfer Characteristics

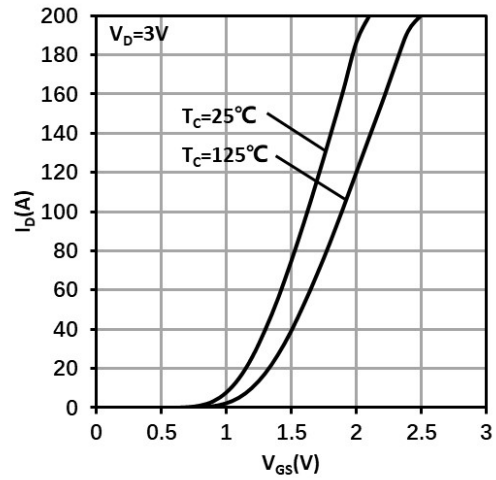


Fig. 7 Typ. Reverse Characteristics ( $V_{GS} \leq 0, T_J = 25^\circ C$ )

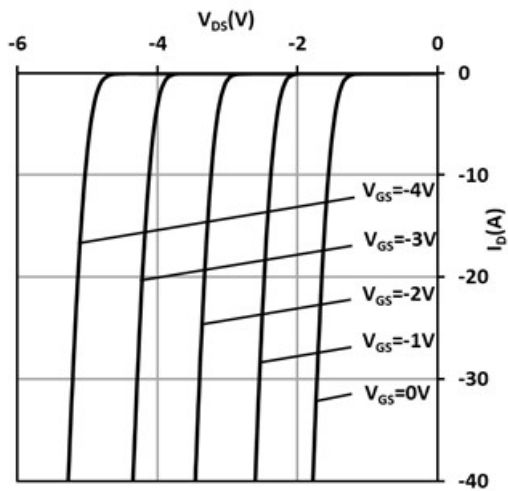


Fig. 8 Typ. Reverse Characteristics ( $V_{GS} \geq 0, T_J = 25^\circ C$ )

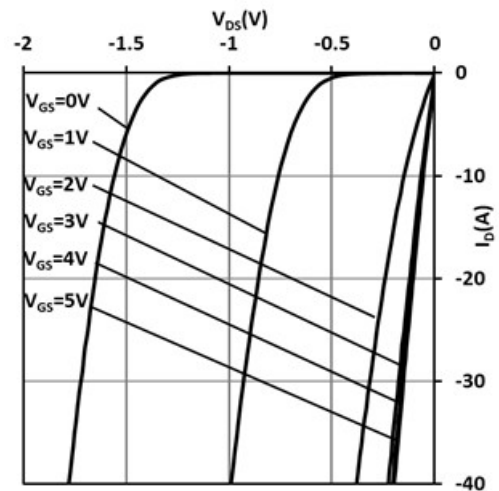




Fig. 9 Typ. Reverse Characteristics  
( $V_{GS} \leq 0, T_J = 125^\circ\text{C}$ )

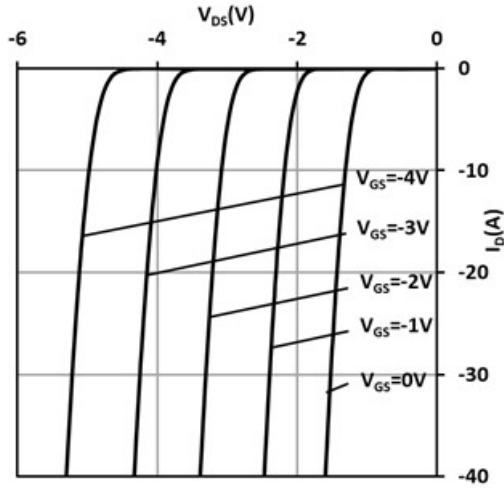


Fig. 10 Typ. Reverse Characteristics  
( $V_{GS} \geq 0, T_J = 125^\circ\text{C}$ )

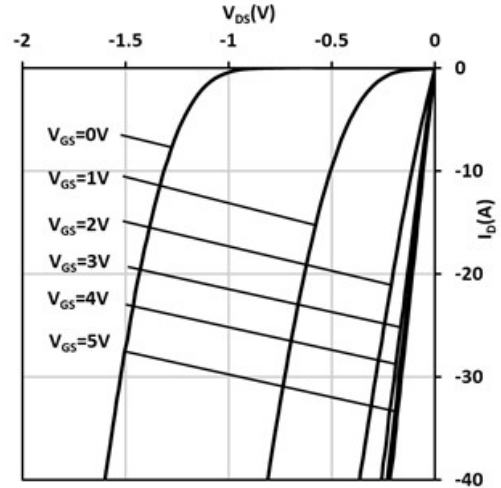


Fig. 11 Typ. Capacitances Characteristics

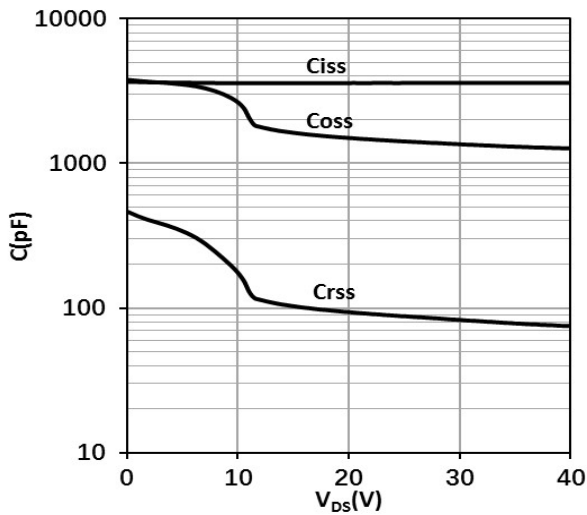


Fig. 12 Typ. Gate Charge

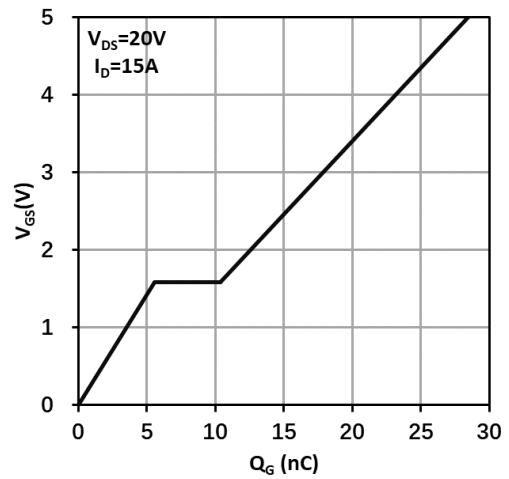


Fig. 13 Normalized Threshold Voltage vs. Temp.

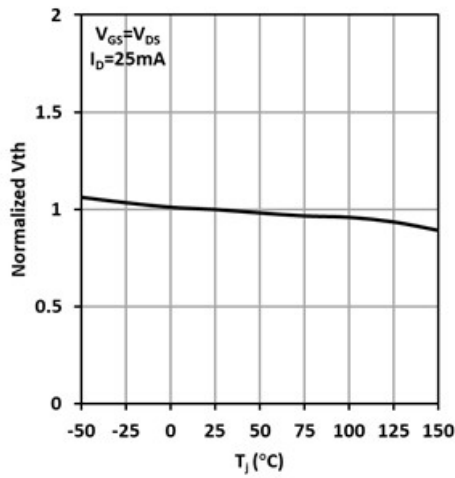


Fig. 14 Output Charge

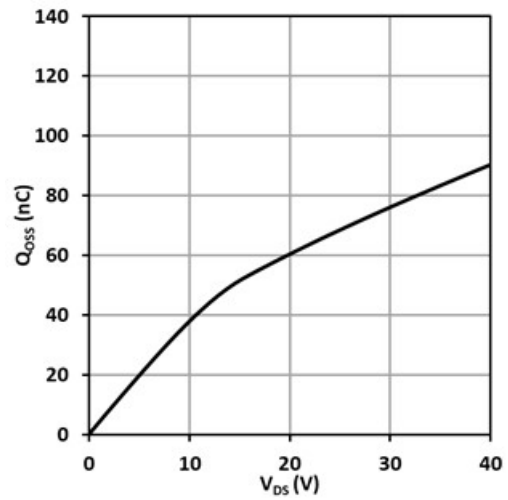


Fig. 15 Output Capacitance Stored Energy

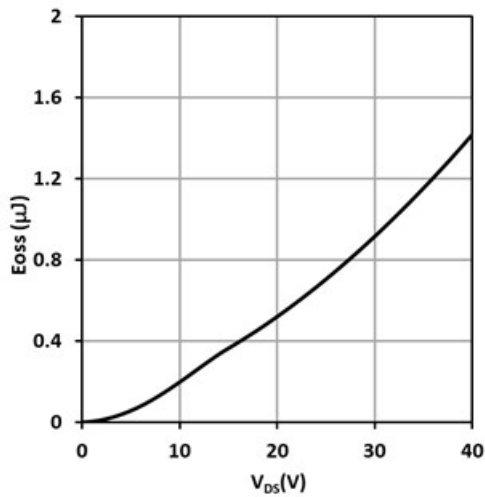


Fig. 16 Power Dissipation

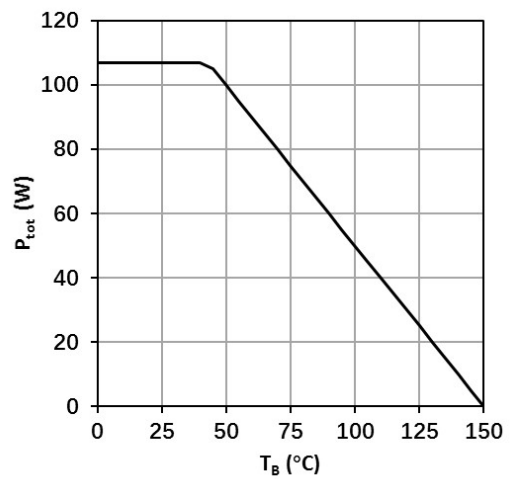


Fig. 17 Safe Operating Area

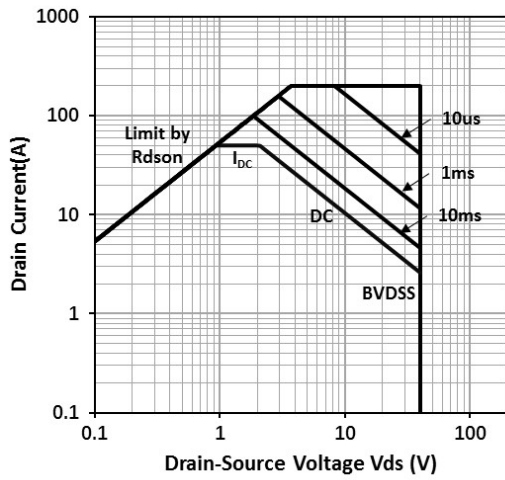
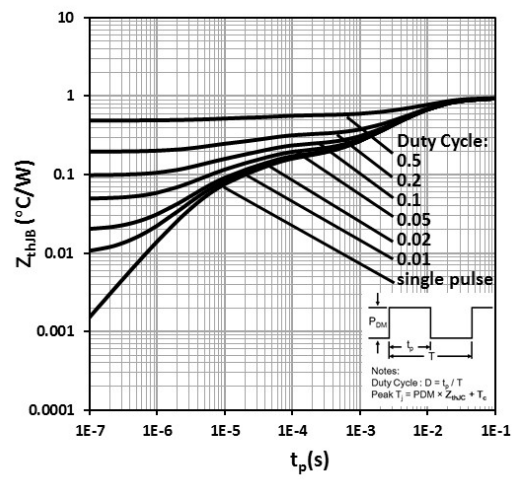
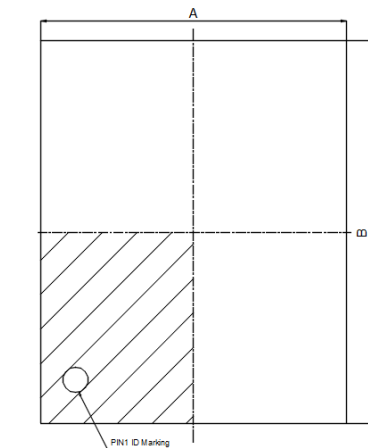


Fig. 18 Max. Transient Thermal Impedance

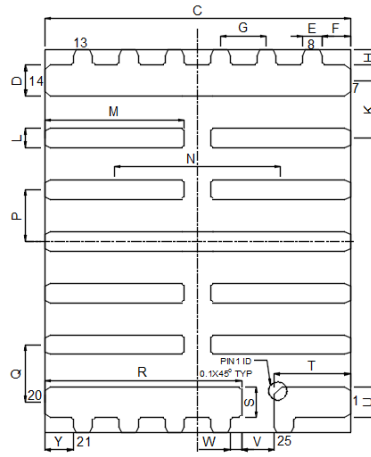


### 10. Package Outlines

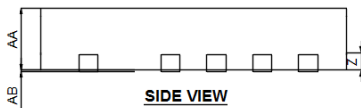
#### Package Reference



TOP VIEW



BOTTOM VIEW



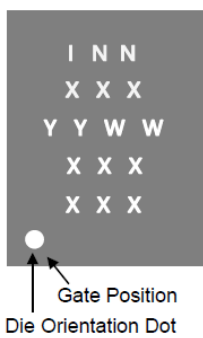
SIDE VIEW

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	4.9	5.0	5.1	
C	3.9	4.0	4.1	
D	0.350	0.400	0.450	
E	0.200	0.250	0.300	11X
F	0.375 REF			2X
G	0.600 BASIC			8X
H	0.200 REF			13X
K	0.750 BASIC			2X
L	0.200	0.250	0.300	9X
M	1.725	1.825	1.925	8X
N	2.175 BASIC			4X
P	0.675 BASIC			8X
Q	0.750 BASIC			2X
R	2.475	2.575	2.675	
S	0.350	0.400	0.450	
T	0.899	0.999	1.099	
U	0.350	0.400	0.450	
V	0.375	0.425	0.475	
W	0.152 REF			
Y	0.375 BASIC			
Z	0.203 REF			
AA	0.650	0.750	0.850	
AB	0	0.02	0.05	

**NOTE:**

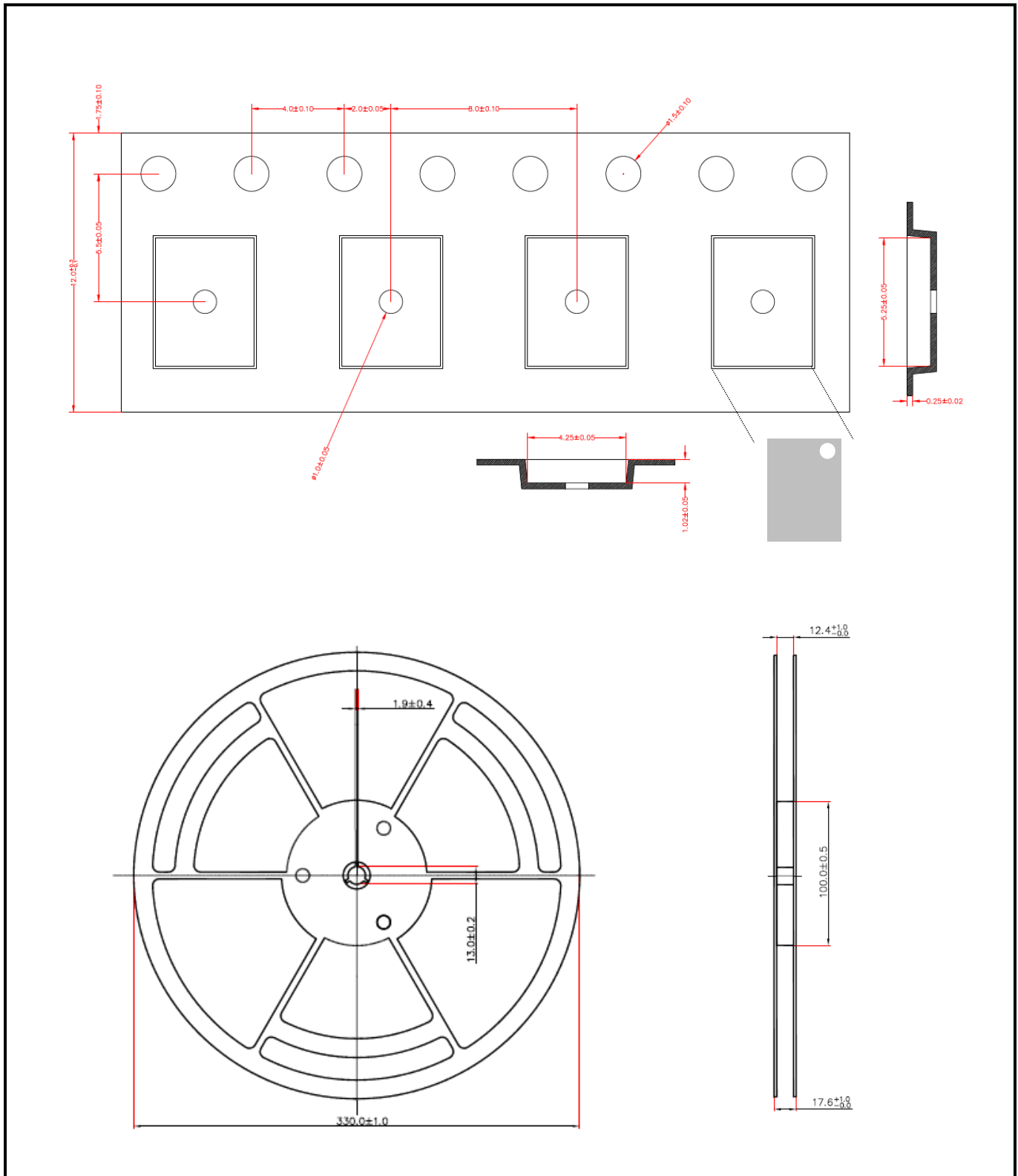
- 1) ALL DIMENSION ARE IN MILLIMETERS.
- 2) BOTTOM VIEW IS FT TESTER SIDE VIEW.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) COMPLIES WITH JEDEC MO-220.
- 5) DRAWING IS NOT TO SCALE.

#### Marking Reference



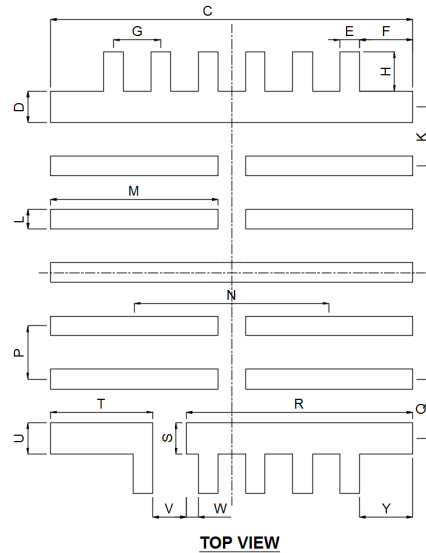
Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot code	XXX
Row 5		XXX

### 11. Reel Information



## 12. Land Pattern

### Recommended Land Pattern

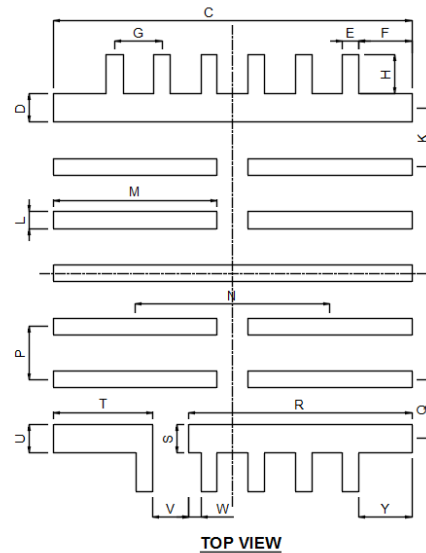


SYMBOL	MILLIMETER	
	NOM	NOTE
C	4.600	
D	0.400	
E	0.250	11X
F	0.675	2X
G	0.600	8X
H	0.500	13X
K	0.750	2X
L	0.250	9X
M	2.125	8X
N	2.475	4X
P	0.675	8X
Q	0.750	2X
R	2.875	
S	0.400	
T	1.299	
U	0.400	
V	0.425	
W	0.152	
Y	0.675	

NOTE:

- 1) LAND PATTERN IS SOLDER MASK DEFINED.
- 2) IT IS RECOMMENDED TO HAVE ON-CU TRACE PCB VIAS.

### Recommended Stencil Drawing



SYMBOL	MILLIMETER	
	NOM	NOTE
C	4.560	
D	0.360	
E	0.210	11X
F	0.675	2X
G	0.600	8X
H	0.500	11X
K	0.750	2X
L	0.210	10X
M	2.085	8X
N	2.475	4X
P	0.675	8X
Q	0.750	2X
R	2.835	
S	0.360	
T	1.259	
U	0.360	
V	0.465	
W	0.152	
Y	0.675	

### 13. Revision History

**Major changes since the last revision**

Revision	Date	Description of changes
1.0	2022-12-01	1.0 Version Setup
1.1	2023-02-23	Update Test Condition In Fig.5, 16-18

## Important Notice

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