ISG3201

1. Features

- 2x 100V, 3.2mohm Emode GaN HEMT with Half Bridge Driver
- 60A continuous current capability
- Zero reverse recovery charge
- Ultra-low on resistance
- Minimum external components. (Driving resistor, bootstrap and Vcc capacitors integrated)
- Reduced Gate Loop Inductance.
- Reduced Power Loop Inductance.
- Easy for power stage layout.
- Independent High-Side and Low-Side TTL Logic Inputs
- High-side floating bias voltage rail operates up to 100 VDC
- Fast Propagation Times (17ns Typical)
- 5mmx6.5mmx1.12mm LGA Package

2. Applications

ISG3201 is suitable for high-frequency Buck converter, half bridge or full bridge converters, Class D audio amplifier, LLC converter and power modules in the following applications:

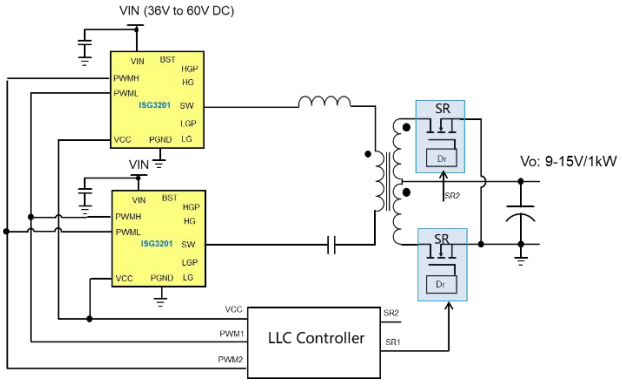
- AI
- Server
- Telecom
- Super Computer
- Motor Drive

3. General description

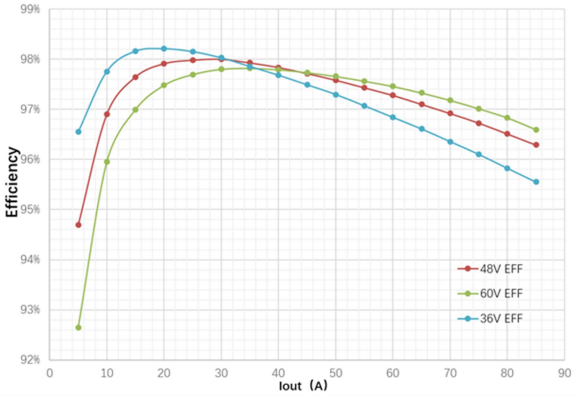
The ISG3201 is a 100V Copak product in Innoscience's SolidGaN family. It integrates two 100V enhancement mode GaN devices with a 100V half-bridge gate driver. ISG3201 employs bootstrap technique for high-side driver voltage and can operate up to 100V. The integrated driver eliminates the external clamping circuit. Besides, turn-on and turn-off resistors, bootstrap and VCC decoupling caps are all integrated which makes the external circuit super simple. Due to excellent internal layout, the associated gate loop and power loop parasitic is reduced significantly, with value much less than 1nH. As a result, ultra-low voltage spike on switch nodes can be achieved. Turn-on speed of the half-bridge GaN HEMTs can be adjusted by an optional resister. The optimized pin layout of ISG3201 optimizes the power flow and simplifies the PCB board layout. ISG3201 employs independent high-side and low-side PWM input, which are usually available from most of GaN controllers. The ISG3201 is available in a compact 5mmx6.5mmx1.12mm LGA package.

4. Typical Application

36V-60V Vin, 4:1 Non-regulated LLC Converter



Efficiency vs Load Current (F_{sw}=1MHz)



5. Absolute maximum ratings

at Tj = 25 °C unless otherwise specified.

All voltages are with respect to PGND pin.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 1 Absolute maximum ratings at T_j = 25 °C

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
Vin	Input Voltage Supply, Vin to GND	100	V
I_D	Continuous current for internal GaN HEMT	60 (*)	A
	Pulsed (25˚C, T_{Pulse} = 100 μs)	230	A
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C
$V_{CC(DC)}$	Supply Voltage (DC)	-0.3 to 6.0	V
$V_{CC(25ns)}$	Supply Voltage (25ns)	-0.3 to 8.0	V
$V_{BST-SW(DC)}$	BST to SW Voltage (DC)	-0.3 to 6.0	V
$V_{BST-SW(25ns)}$	BST to SW Voltage (25ns)	-0.3 to 8.0	V
$V_{SW(DC)}$	SW pin Voltage	-0.3 to 105	V
$V_{SW(25ns)}$	SW pin Voltage (25ns)	-5V to 108	V
$V_{BST-PGND}$	BST to PGND Voltage	-0.3 to V_{SW}+6.0	V
V_{HGP}, V_{HG}	HGP, HG pin Voltage	V_{SW}-0.3 to V_{BST}+0.3	V
V_{LGP}, V_{LG}	LGP, LG pin Voltage	-0.3 to 6.0	V
PWMH, PWML	PWMH, PWML pin Voltage	-0.3 to 6.0	V

(*) Ideal thermal condition. In real application the current capability depends on system thermal design.

6. Recommended Operating Conditions

Table 2 Recommended operating Conditions

Parameter	Min	Max	Unit
Vin		80	V
VCC	4.5	5.5	V
PWMH, PWML	0	5.5	V
V_{SW}	-4	100	V
BST	SW+4.5	SW+5.5	V
SW Slew Rate		50	V/ns
Operating Junction Temperature T_J	-40	125	˚C

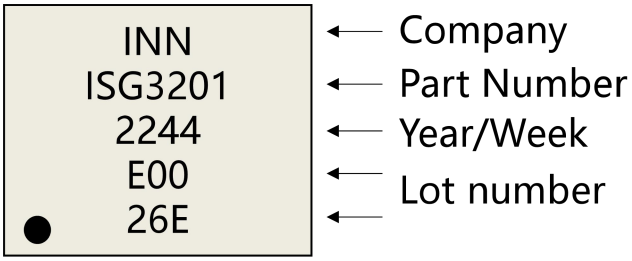
7. Ordering information

Table 3 Ordering information

PART NUMBER	PAD FINISH[1] (Note 1)	TOP MARKING	PACKAGE TYPE	MSL RATING
ISG3201	SAC305 (RoHS)	See Below	LGA	3

1. Pad or ball finish code is per IPC/JEDEC J-STD-609.

Top Marking



8. Pinout description

Package top view is shown as follows:

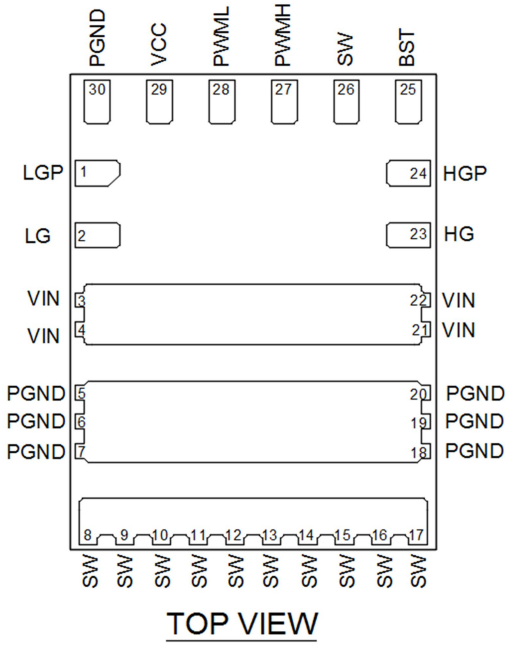


Table 4 Pinout description

Pin Number	Symbol	Pin Type	Description
1	LGP	Output	Low side gate driver source-current output. An optional resistor between LGP and LG can be employed to adjust turn-on speed of low side GaN HEMT. See in Apps info for more details.
2	LG	Output	Low side gate terminal.
3-4,21-22	VIN	Power	Input voltage supply. Add high quality decoupling cap between VIN and PGND with minimum loop.
5-7,18-20, 30	PGND	GND	Power ground.
8-17	SW	Output	Switching node.
23	HG	Output	High side gate terminal.
24	HGP	Output	High side gate driver source-current output. An optional resistor between HGP and HG can be employed to adjust turn-on speed of high side GaN

			HEMT. See in apps info for more details.
25	BST	Output	High side gate driver bootstrap rail, bootstrap cap is built in internally and no decoupling cap is required between BST and SW pin.
26	SW	Output	Switching node. SW waveform can be monitored.
27	PWMH	Input	High side driver PWM input. Can be floating if not used.
28	PWML	Input	Low side driver PWM input. Can be floating if not used.
29	VCC	Input	External 5V Driver supply. No decoupling cap to PGND is required.

9. Electrical specification

V_{CC} =5V, T_A = 25°C for typical value, unless otherwise noted. For further information, contact Innoscience sales office.

Table 5 Electrical specification

Parameter	Symbol	Min.	Typ.	Max.	Units	Note/Test Condition
VCC SUPPLY						
I_{VCC} Quiescent Current				100	uA	PWMH=PWML=0
I_{VCC} Operation Current				30	mA	
V_{CC} Under Voltage Lockout Threshold Rising	VCC_{VTH}		4	4.35	V	
V_{CC} Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}		300		mV	
PWM INPUT						
PWM Logic High Voltage	V_{H_PWM}	2.1			V	
PWM Threshold Hysteresis	V_{HYS_PWM}		400		mV	
PWM Logic Low Voltage	V_{L_PWM}			1.3	V	
PWM input pull-down resistance	R_{PWM_IN}		200		kΩ	
High and Low-side Gate Driver						
Peak source current (*)	I_{SOURCE}		1.7		A	V_{HG-SW}=0V, V_{LG-LS}=0V
Peak sink current (*)	I_{SINK}		5.2		A	V_{HG-SW}=5V, V_{LG-LS}=5V
Source Resistance	R_{SOURCE}		1.3		Ω	I_{SOURCE} =100mA, 5V
Sink Resistance	R_{SINK}		0.2		Ω	I_{SINK} =100mA, 5V
High and Low-side Gate Driver Timing Characteristics (*)						
HGP Rise Time (0.5V-4.5V)	T_{R_SW}		10		ns	3.3nF load, VCC=5V
HG Fall Time (4.5V-0V)	T_{F_SW}		3		ns	3.3nF load, VCC=5V
LGP Rise Time (0.5V-4.5V)	T_{R_LS}		10		ns	3.3nF load, VCC=5V
LG Fall Time (4.5V-0.5V)	T_{F_LS}		3		ns	3.3nF load, VCC=5V
HGP Turn-On propagation Delay	t_{HPH}		17		ns	3.3nF load, VCC=5V, PWMH rising to HGP rising
HG Turn-Off propagation Delay	t_{HPL}		17		ns	3.3nF load, VCC=5V, PWMH rising to HGP rising
LGP Turn-On propagation Delay	t_{LPH}		17		ns	3.3nF load, VCC=5V, PWMH rising to HGP rising
LG Turn-Off propagation Delay	t_{LPL}		17		ns	3.3nF load, VCC=5V, PWML falling to LG falling
LGP on & HG off delay matching	t_{OFF_M}		1.5		ns	
LG off & HGP on delay matching	t_{ON_M}		1.5		ns	
Minimal input PWM pulse	t_{PWM_MIN}		10		ns	
Minimal gate output pulse	t_{GATE_MIN}		13		ns	
GaN FET						
Drain-to-Source Voltage	BV_{DSS}	100			V	V_{GS} = 0 V, I_D =400μA

Drain-Source Leakage	I_{DSS}		80	350	μA	V_{GS} = 0 V, V_{DS} = 80 V
Gate-to-Source Forward Leakage(25°C)	I_{GSS}		20	5000	μA	V_{GS} = 5 V
Gate-to-Source Forward Leakage(125°C)			0.6	9	mA	V_{GS} = 5 V
Gate-to-Source Reverse Leakage			60	400	μA	V_{GS} = -4 V
Gate Threshold Voltage	$V_{GS(TH)}$	0.8	1.1	2.5	V	V_{DS} = V_{GS}, I_D = 9 mA
Drain-Source On Resistance	$R_{DS(on)}$		2.4	3.2	mΩ	V_{GS} = 5 V, I_D = 25 A
Source-Drain Forward Voltage	V_{SD}		1.5		V	I_S = 0.5 A, V_{GS} = 0 V
Input Capacitance	C_{ISS}		1000		pF	V_{GS} = 0 V, V_{DS} = 50 V
Output Capacitance	C_{OSS}		460			V_{GS} = 0 V, V_{DS} = 50 V
Reverse Transfer Capacitance	C_{RSS}		8.2			V_{GS} = 0 V, V_{DS} = 50 V
Energy Related C_{OSS}	$C_{OSS(ER)}$		700			V_{GS} = 0 V, V_{DS} = 0 to 50 V
Time Related C_{OSS}	$C_{OSS(TR)}$		1020			V_{GS} = 0 V, V_{DS} = 0 to 50 V
Gate resistance	R_G		2.2		Ω	
Total Gate Charge	Q_G		9.2	12	nC	V_{GS} = 5 V, V_{DS} =50V,I_D = 25 A
Gate-to-Source Charge	Q_{GS}		1.9			V_{DS} = 0V to 50 V, I_D = 25 A
Gate-to-Drain Charge	Q_{GD}		1.7			V_{DS} = 0V to 50V, I_D = 25 A
Gate Charge at Threshold	$Q_{G(TH)}$		1.1			V_{DS} = 0V to 50V, I_D = 25 A
Output Charge	Q_{OSS}		50			V_{GS} = 0 V, V_{DS} = 0 to 50V

(*) Guaranteed by design or characterization data, not tested in production.

10. Thermal characteristics

Table 6 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction to case Top	$R_{thJC-TOP}$	27	°C/W	Determined by simulation per JESD51 conditions
Thermal resistance, junction to case Bottom	$R_{thJC-BOT}$	7.7	°C/W	Determined by simulation per JESD51 conditions
Thermal resistance, junction to ambient	R_{thJA}	48	°C/W	Determined by simulation per JESD51 conditions
Reflow soldering temperature	T_{sold}	≤260	°C	

*According to standards defined in JESD51 and JESD51-1, thermal characteristic of the package is simulated.

11. ESD ratings

Table 7 ESD ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Human Body Model (per JESD22-A114)	HBM	±1000	V	Human Body Model (per JESD22-A114)
Charged Device Model (per JESD22-C101F)	CDM	±500	V	Charged Device Model (per JESD22-C101F)

12. Typical Performance Characteristics

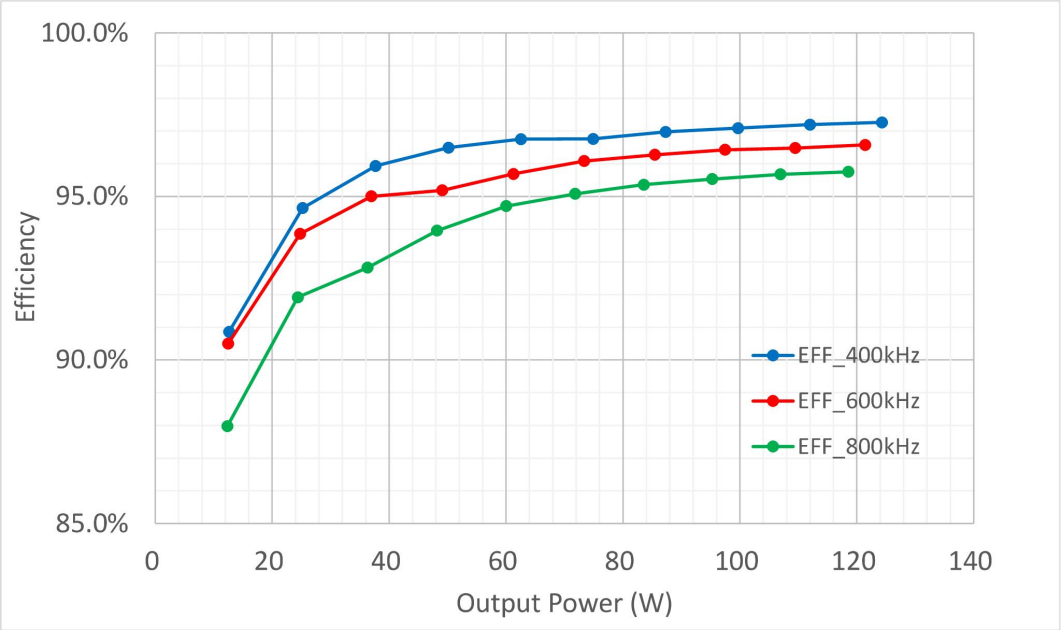


Fig. 1 Typical Efficiency Vs. Output Power for Buck Converter

Buck Converter: Vin=48V, Vo=12V, R_{gon}=5Ω, R_{goff}=0Ω. T_{dead}=10ns. L=2.2uH/0.7mΩ. Based on Inno Demo Board: INNEHB100B1. Refer to Figure 4 for a simplified application schematic.

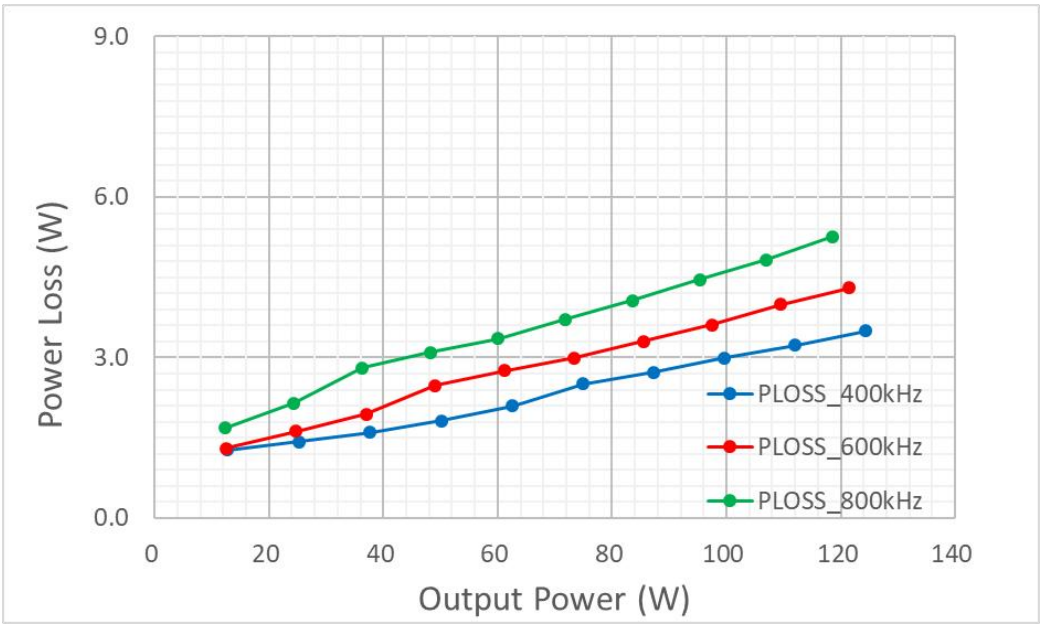


Fig. 2 Power Loss Vs. Output Power for Buck Conveter

Buck Converter: Vin=48V, Vo=12V, R_{gon}=5Ω, R_{goff}=0Ω. T_{dead}=10ns. L=2.2uH/0.7mΩ. Based on Inno Demo Board: INNEHB100B1. Refer to Figure 4 for a simplified application schematic.

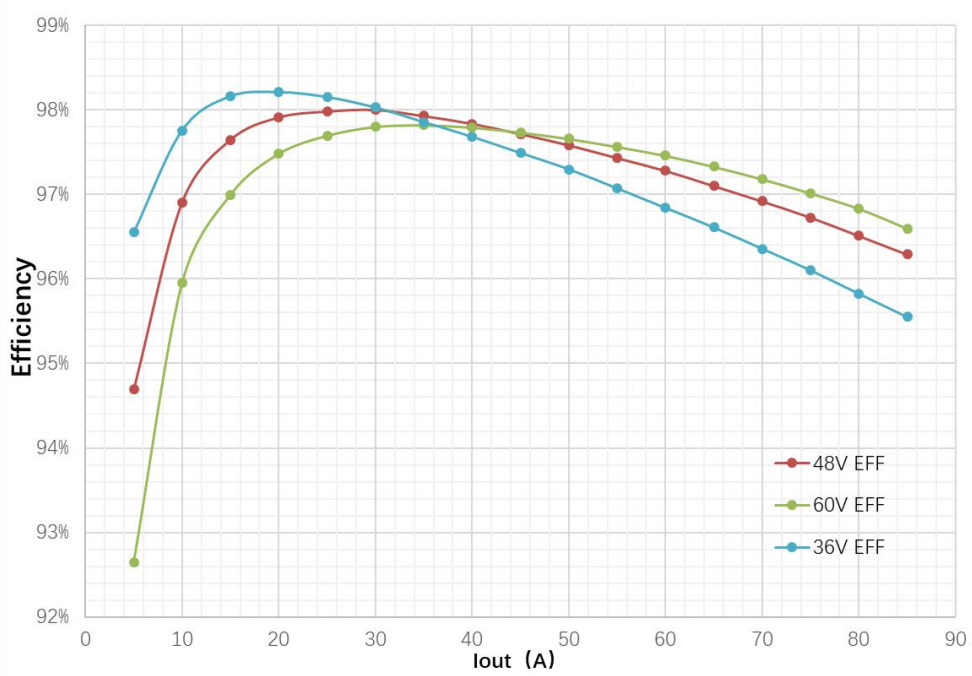


Fig. 3 Typical Efficiency Vs. Output Current for LLC Converter

LLC Converter: 4:1 Non-regulated, R_{gon}=4Ω, F_{sw}=1MHz, L_p=3.4uH. T_{dead}=53ns. Cr=3100nF. Based on Inno Demo Board: INNDDD1K0A1. Refer to Figure 5 as a simplified application schematic.

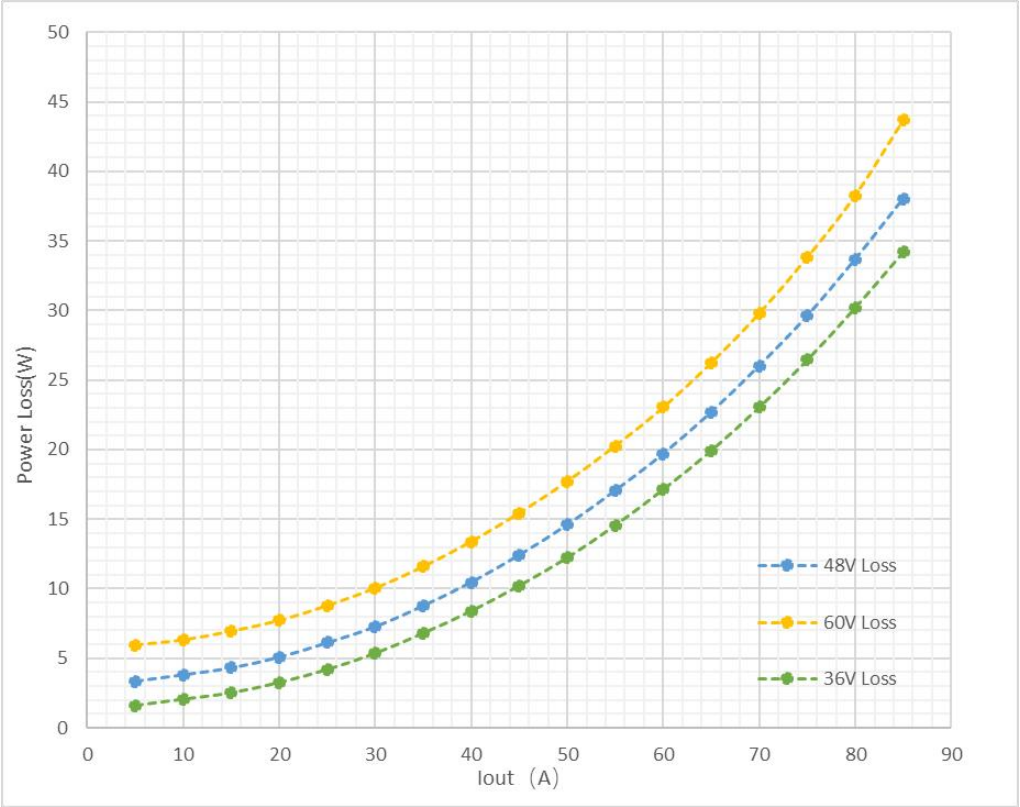


Fig. 4 Power Loss Vs. Output Current for LLC Converter

LLC Converter: 4:1 Non-regulated, R_{gon}=4Ω, F_{sw}=1MHz, L_p=3.4uH. T_{dead}=53ns. Cr=3100nF. Based on Inno Demo Board: INNDDD1K0A1. Refer to Figure 5 as a simplified application schematic.

13. Block Diagram

Block Diagram of ISG3201 is shown as Figure 1. A half-bridge GaN driver and two 100V GaN HEMTs are integrated. Besides, Vcc decoupling capacitor, Bootstrap capacitor, internal 20Ω turn-on resister for both GaN HEMTs are also integrated. Turn-on speed can be adjusted by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT.

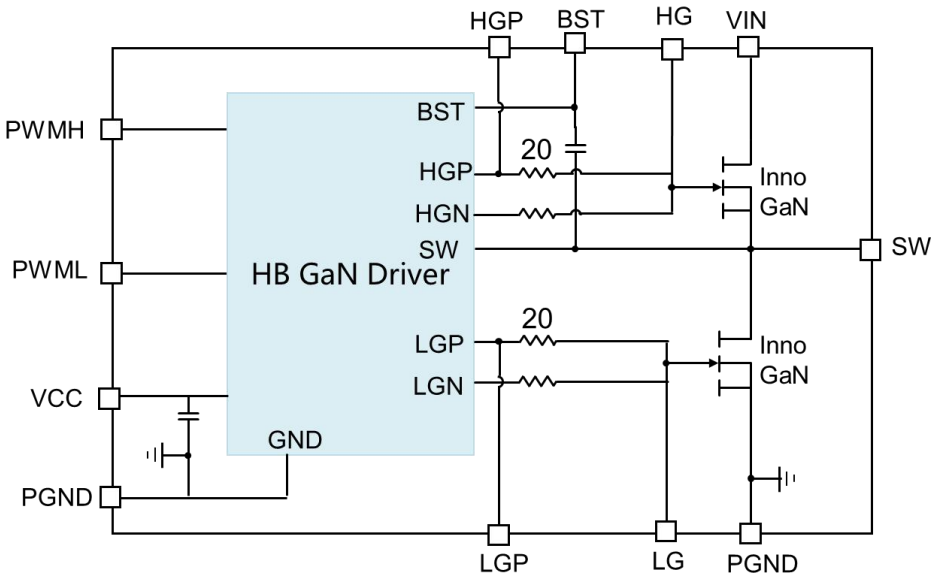


Figure 1. Block diagram of ISG3201

14. Operation and Applications Information

The ISG3201 is designed as a fully integrated GaN Half-bridge power stages for multiple applications in Data Center, Server, Super computer, motor drive and class D audio systems. It is one of leading products in Innoscience's SolidGaN families. ISG3201 is small-footprint, easy for design and layout and serve as "drop-in" solution for board power. ISG3201 combines world-class GaN performance from Innoscience with high performance half-bridge driver specifically designed for GaN. Bootstrap capacitor, driving resistors and Vcc decoupling caps are all integrated into ISG3201 which significantly simplifies the application circuit. The optimized pinout structure makes the layout ultra easy while the parasitic is reduced significantly, i.e. gate loop and power loop paracitics. As a result, voltage spike of SW node is very small which enhances the reliability of the system.

14.1 PWM Input and Output

The PWMH and PWML are logical inputs which can with stand voltage up to 5.5V and independently controlled. PWMH controls the high-side FETs and PWML controls low-side FETs of the same bridge. Please refer to Table 8 as below. Therefore, the users must avoid shoot through by setting sufficient dead time, t_{d1} and t_{d2}, between PWMH and PWML, as illustrated in Figure 2.

Table 8: PWMH and PWML True Table

PWMH	PWML	HG	LG	Comment
High	Low	High	Low	Top HEMT On
Low	High	Low	High	Bottom HEMT On
Low	Low	Low	Low	Both HEMT Off
High	High	High	High	Both HEMT On

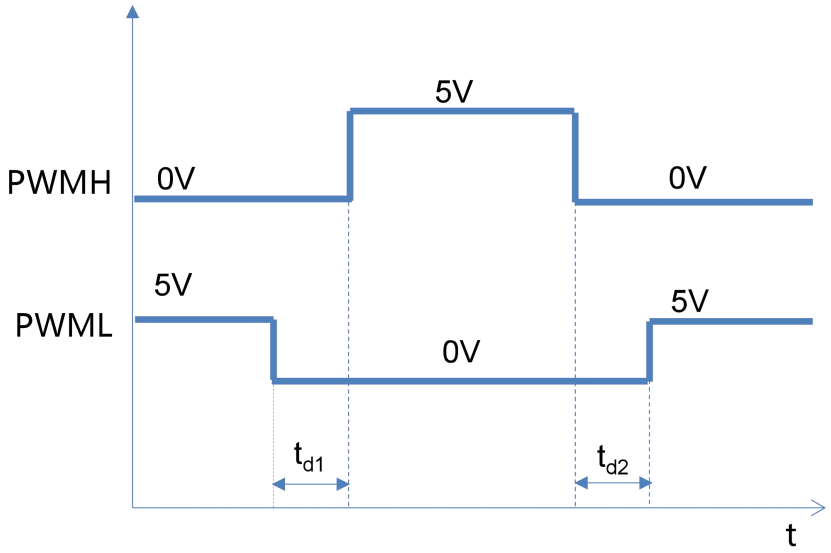


Figure 2. Dead-time Illustration diagram

ISG3201 employs a gate driver which separate the gate turn-on and turn-off outputs. A default internal 20Ω turn-on resister for both GaN HEMTs are integrated. Turn-on speed can be increased by an optional resistor between HGP(LGP) pin and HG(LG) pin for top (bottom) GaN HEMT. The total effective resistance is the parallel of the external resistor and 20Ωinternal resistor.

14.2 UVLO Protection

When VCC voltage is lower than the threshold voltage of VCC_{VTH}, both PWMH and PWML are ignored. When VCC>VCC_{VTH} both HG and LG are working. Please refer to Table 8.

14.3 BOOTSTRAP Clamping inside ISG3201

Due to the intrinsic feature of enhancement mode GaN FETs, the source-to-drain voltage of the bottom switch, is usually higher than a diode forward voltage drop when the gate is pulled low. For example, When V_{gs}=0V and the source to drain current is 15A, source-to-drain voltage is around 1.5V. This will cause negative voltage on SW pin. Moreover, this negative voltage transient will be even worse, considering layout and device drain /source parasitic inductances. With high side driver using the floating bootstrap configuration, negative SW voltage can lead to an excessive bootstrap voltage which can damage the high-side GaN FET. ISG3201 employ new charging logical, only when PWML=1, the BST-SW voltage will be charged from VCC. There is no current path from VCC to BST when

PWML=0, so the BST-SW voltage should <=VCC. Besides, an active circuit clamps BST-SW voltage from exceeding (1.05*VCC).

An internal bootstrap cap is already integrated into ISG3201. Additional bootstrap cap can also been added between BST and SW pin, if necessary. To ensure reliable operation of bootstrap cap charging, the pulse width of PWML=1 should be larger than 50ns.

14.4 Layout Recommendation

The GaN HEMTs feature very small input capacitance: i.e. a very small gate capacitance and miller capacitance. Therefore, The GaN HEMTs can operate with very-fast-speed switching: i.e. high dv/dt and high di/dt. In order to avoid the voltage and current spike caused by high dv/dt and high di/dt, the parasitic of the gate driving loop and power loop must be reduced by proper layout technique.

ISG3201 employs an excellent layout on internal substrate to reduce the gate driving loop and power loop: (1) the driver has been placed very close to the GaN HEMTs to minimize the loops of parasitic inductance and reduce the noise on the gate loop. (2) the bootstrap capacitor is integrated in the module and the distance between BST and VCC to the driver has been minimized which avoids the possible high peak current during recharging time. (3) the distance between high-side GaN FET and low-side GaN FET has been minimized to avoid excessive negative voltage to the driver caused by the parasitic inductance between high-side GaN HEMT and low-side GaN HEMT.

Although the optimized pinout of ISG3201 simplifies the power stage layout significantly, to fully utilize the benefit of ISG3201, A good power board layout is still necessary.

The layout guidelines are as follows:

1. The optional resistor between HGP(LGP) pin and HG(LG) pin to adjust the turn-on speed of the GaN HEMT should be placed close to ISG3201.

2. The optional VCC decoupling capacitor should be placed close to ISG3201.

3. The power input decoupling caps should be placed close to Vin bar and PGND bar. One 4-layer layout example is shown as Figure 3. 2-layer board design is also possible thanks to the optimized ISG3201 pinout.

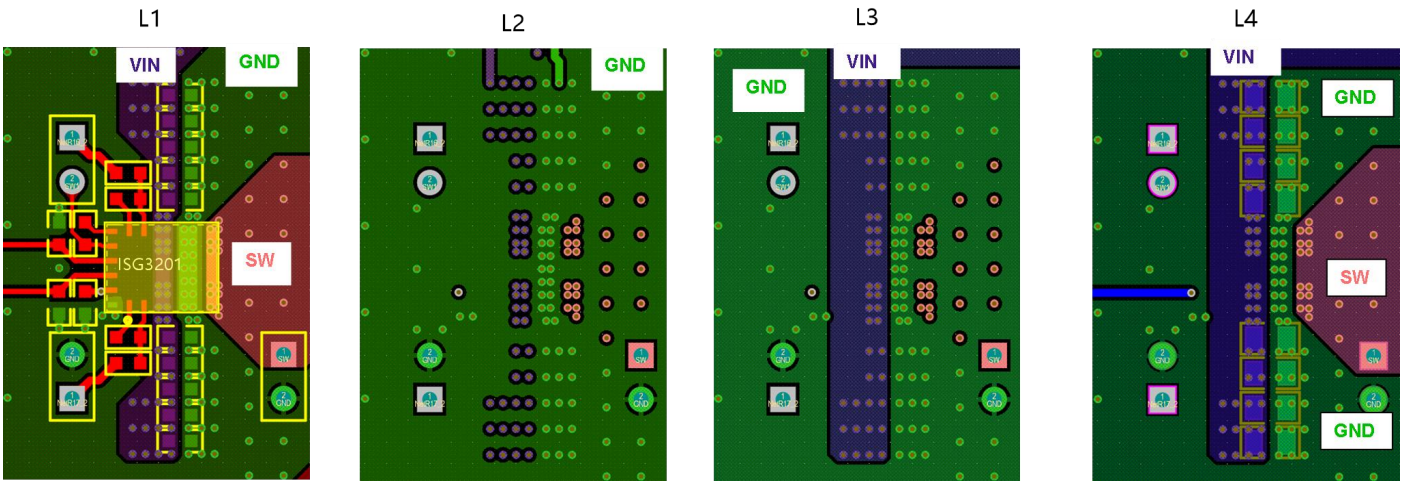


Figure 3. 4-Layer Layout Example

The typical ISG3201 application circuit is shown in Figure 4 for Buck converter, Figure 5 for LLC converter, and Figure 6 for 500W continuous/1000W pulsed power capability motor driver.

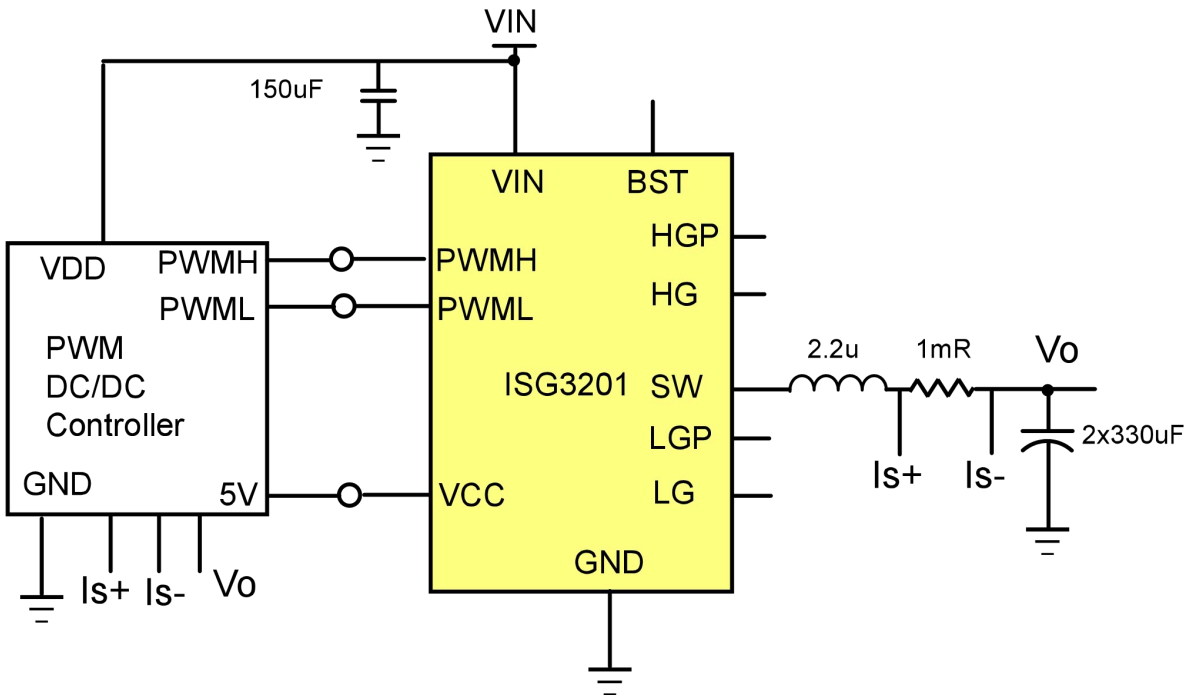


Figure 4. 36Vin to 80Vin, 12Vo/300W Buck Converter

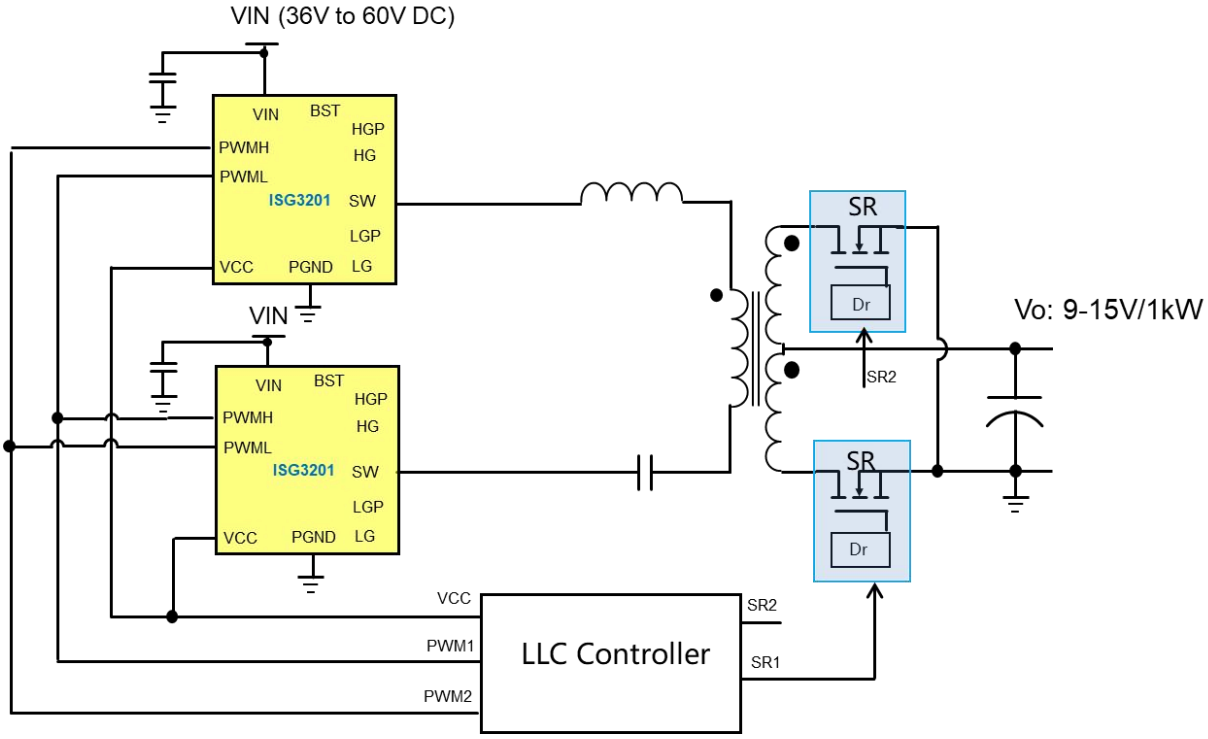


Figure 5. 36V-60V Vin, 9V-15V Vo /1kW LLC Resonant Converter

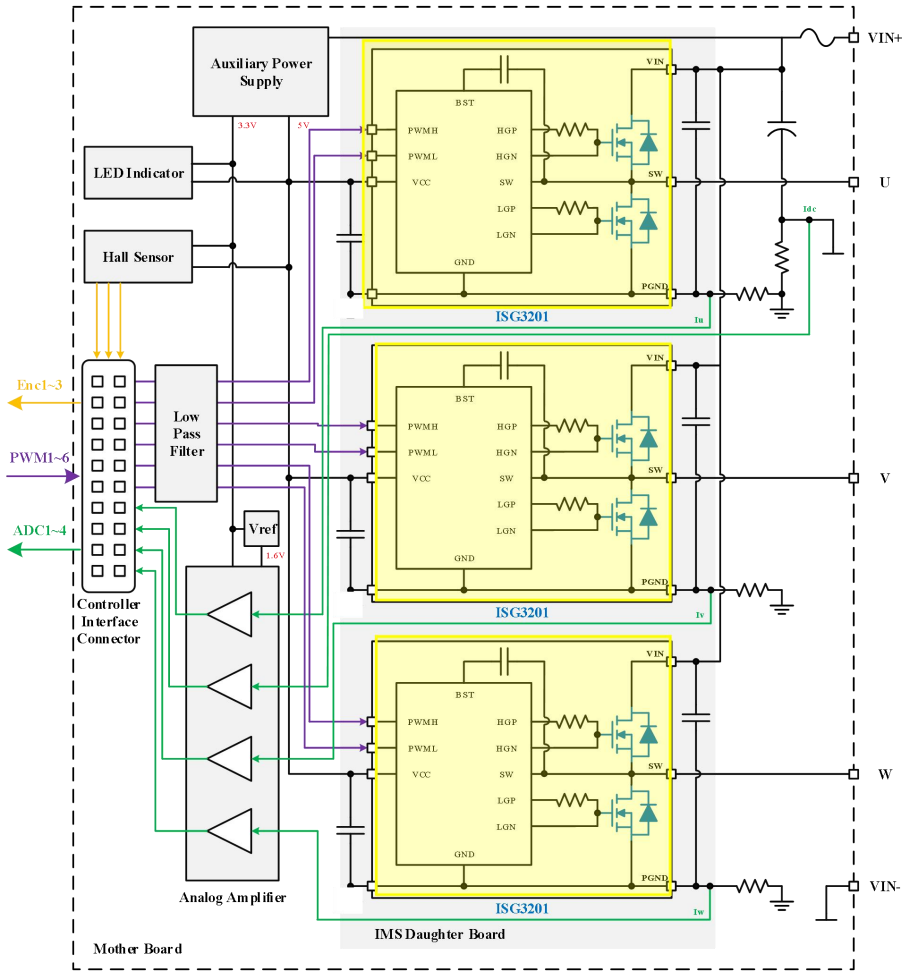


Figure 6. 500W Continuous/1000W Pulse Power Capability Motor Driver

15. Package Information

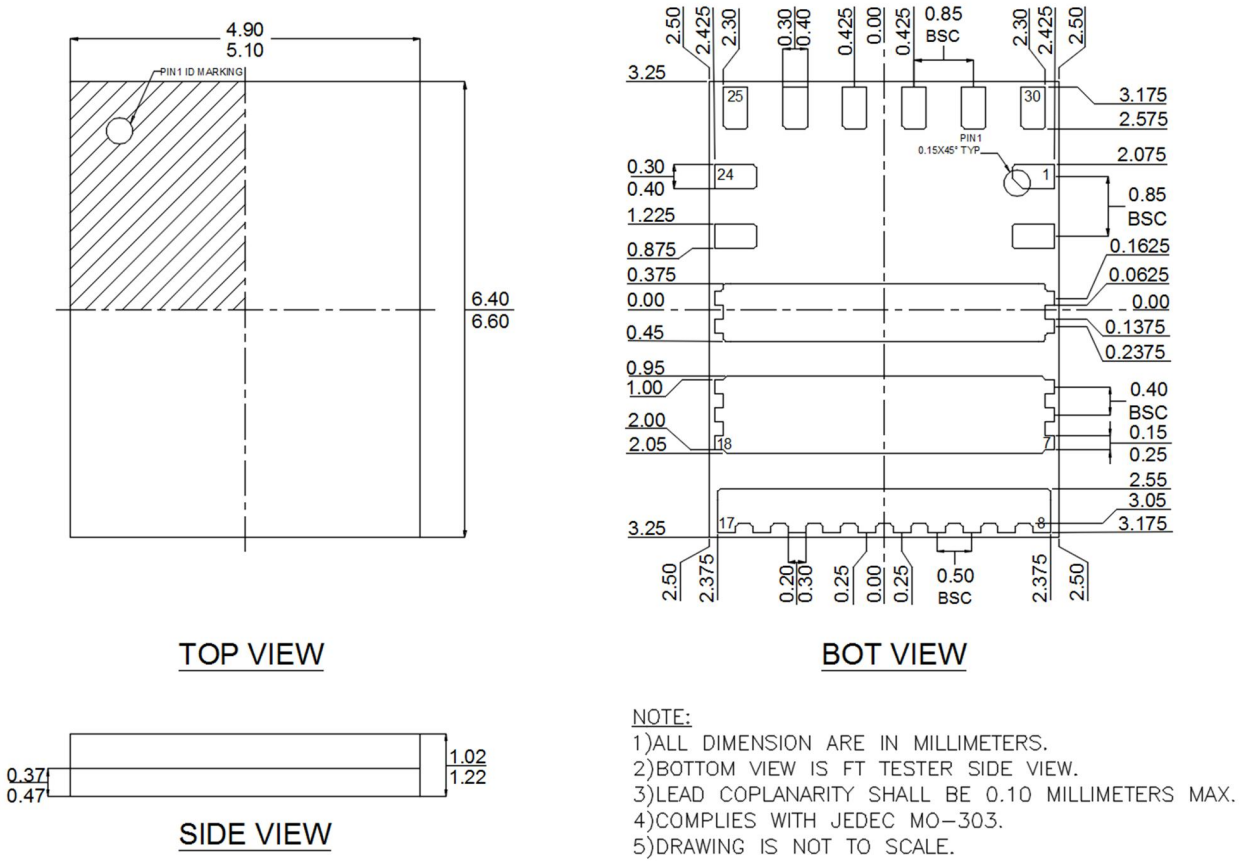
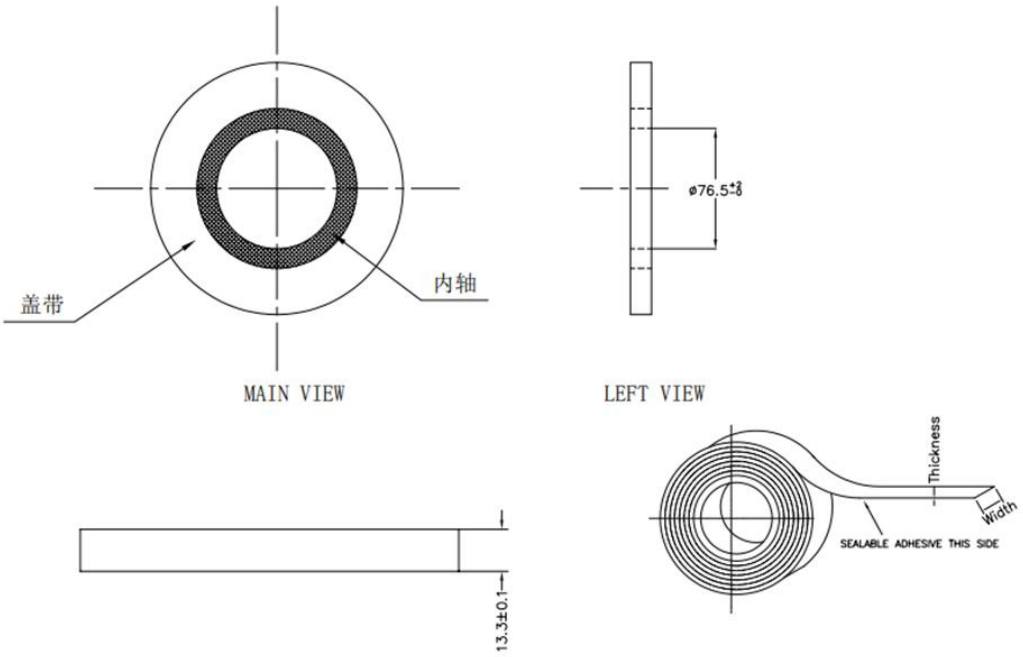


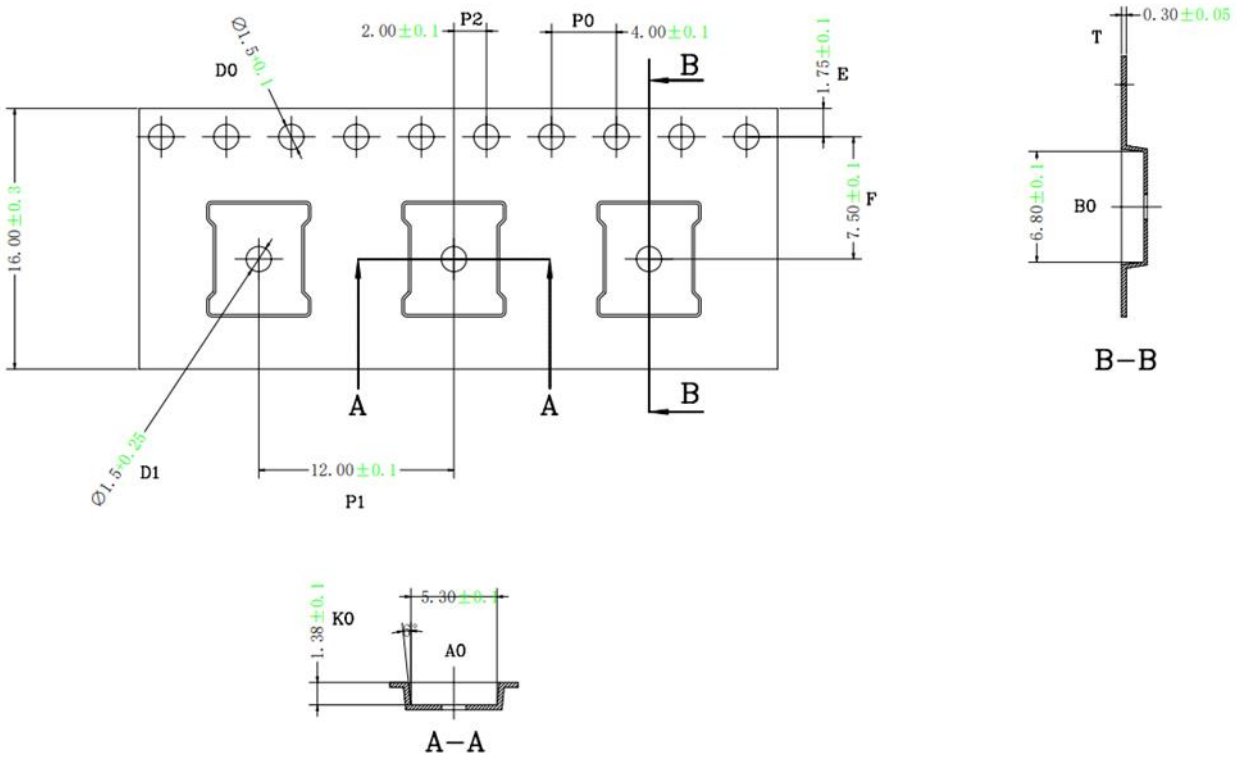
Figure 7. Package Information

16. Tape and Reel Information



TECHNOLOGY SPECIFICATION[技术要求]
1. COVER TAPE COLOR:TRANSPARENT.[盖带颜色：透明]
2. COVER TAPE THICKNESS: 48±5um.[盖带厚度：48±5微米]
3. THE MATERIAL:PS[材质：聚乙烯]
4. SURFACE RESISTANCE: $1\times10^{5}\sim1\times10^{11}\Omega$.[表面电阻：$1\times10^{5}\sim1\times10^{11}\Omega$]
5. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.
[禁止使用长电科技规定的一级环境管理物质]

Figure 8. Tape Information



TECHNOLOGY SPECIFICATION[技术要求]
1. CARRIER TAPE COLOR:BLACK.[载带颜色为黑色]
2. THE MATERIAL:PS [材质：聚苯乙烯]
3. SURFACE RESISTANCE $1X10^4$～$1X10^9$OHMS.[表面电阻为$1X10^4$～$1X10^9\Omega$]
4. MOLD# LGA（5×6.5）.[载带规格LGA（5×6.5）]
5. COVER TAPE WIDTH:13.3±0.1mm. [配套13.3±0.1mm宽盖带]
6. TOLERANCE:X.X ±0.20 X.XX±0.10 [未注明公差参考：X.X±0.2 X.XX±0.10]
7. COVER TAPE COLOR:TRANSPARENT [盖带颜色无色透明]
8. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.
[禁止使用长电科技规定的一级环境管理物质]

Figure 9. Reel Information

17. Recommended Land Pattern.

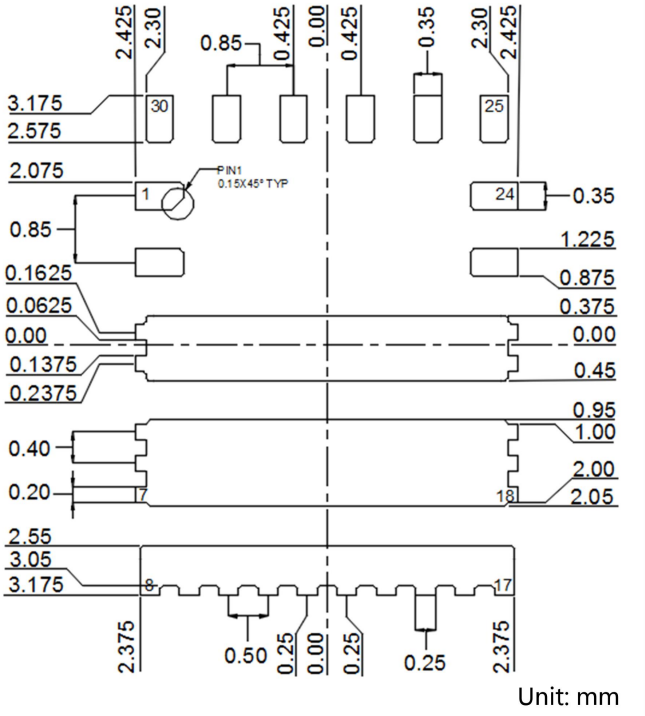


Figure 10. Recommended Land Pattern

18. Revision History

Major changes since the last revision

Revision	Date	Description of changes
DS 1.0	2023-06-28	Final datasheet at product release – for MP

Important Notice